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The Silicon Vertex Detector of the Collider Detector at Fermilab

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The Silicon Vertex Detector of the Collider Detector at Fermilab

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Abstract

A silicon microstrip vertex detector has been constructed and installed in the Collider Detector at Fermilab. The device has been designed to operate at a hadron collider. It began collecting data in May of 1992 and has functioned within specification. Technical details are presented on all aspects of the system and its performance.

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Contents

1 Introduction

Among the issues of particular interest to high energy physics are the existence and mass of the top quark and the masses, decays, and production dynamics of b hadrons. These issues can be addressed, at least in part, by experiments performed at hadron colliders where the decay products of b hadrons are identified or reconstructed. In the first case, b hadrons should be produced in the decay of top. Their presence, in these typically complex final states, can be used to reject backgrounds. In the second case, b hadrons are produced copiously and directly at low p_t in hadron colliders. For example at the Fermilab Tevatron Collider the cross section to produce a b particle with $p_t > 10$ GeV/c is ≈ 1.5 μbarn. Consequently hadron colliders can be good sources of b hadrons for study.

A significant distinguishing feature of b hadron decays is their relatively long lifetime ($c\tau \approx 430$ μm). This implies the decay may be tagged and also the flight path measured with a sufficiently precise tracking detector. In an attempt to exploit the potential for interesting physics using b hadrons, a detector designed to resolve the event vertices in $\bar{p}p$ collisions at high energy has been constructed and installed in the Collider Detector at Fermilab (CDF) [4]. This device acquired data between May of 1992 and June of 1993 and functioned well. The capability of precise vertex tracking at CDF figures significantly into a number of physics analyses [1],[2], [3]. This detector utilizes silicon microstrip technology to achieve asymptotic impact parameter resolutions of order 10 μm and is therefore referred to as the Silicon Vertex Detector (SVX). In this paper we present a comprehensive description of this device, its components, construction, subsystems, online and offline performance, and radiation damage.

2 Overview and Specification

The Collider Detector at Fermilab was first constructed and commissioned in the mid-1980's for use in the study of high transverse momentum phenomena. The detector, as originally configured, is described in detail in a series of articles published in NIM [4]. The addition of the Silicon Vertex Detector described here is an upgrade to the original CDF tracking system. The feature of the original tracking system most relevant to the design and operation of the SVX is the magnetic spectrometer. This is comprised of a 1.41 Tesla superconducting solenoid enclosing a cylindrical drift chamber, (the CTC[5]) of outer radius 1.32 m. This central tracking chamber contains both axial and stereo wire layers but tracks with higher resolution in the $r\phi$ (transverse) plane. The performance of this chamber in conjunction with the SVX is described in Section 14. Figure 1 shows the overall layout of the CDF central detectors including the SVX.

The Silicon Vertex Detector for CDF was designed to operate in the environment imposed by the Fermilab Tevatron Collider[6]. The consequences of this will be discussed in this section where we describe the design specifications of the device. Table 1 summarizes the operating parameters of the Tevatron Collider. Figure 2 is a view of the SVX, and Table 2 summarizes its features. The organization of this section mirrors the body of the paper.

In developing this new detector for CDF, a number of general principles and specifications were followed. These led to various technical tradeoffs and design choices. These basic items were as follows:

- Detector performance should match the requirements of b decay reconstruction.

Beam:	proton–antiproton
Beam Energy:	900 GeV/beam
Luminosity:	$10^{30} - 10^{31}\ cm^{-2}sec^{-1}$
Bunches/Beam:	6
Bunch Spacing:	3.5 μs
Collision Region RMS:	30 cm
Beam Spot:	$\approx 40\ \mu$m
Beam Pipe:	1.5 in. diameter

Table 1: 1992–1993 Tevatron Collider operating parameters.

- The detector should be extended longitudinally to cover as much of the Tevatron luminous region as possible.
- The detector should have sufficient redundancy and granularity to handle complex events.
- The inner radius should be as small as possible to obtain the best impact parameter resolution.
- The mass of the detector should be minimized to reduce multiple scattering and photon conversions.
- The detector should function with the existing CDF tracking and data acquisition systems.
- Technological choices should be geared towards reliability and not an excessive use of new or untested concepts.

These principles led to a design which favoured redundant measurements of tracks in the $r\phi$ (transverse) plane over full three dimensional tracking. Consequently we opted to install four concentric cylindrical layers of single sided silicon detectors rather than utilize the newer double sided detector technology. In addition we opted to concentrate effort on developing readout and data acquisition electronics which could efficiently filter out empty channels as early as possible. We wanted the event size and readout time to be determined by occupancy rather than channel count.

2.1 Mechanical Configuration

At the Tevatron Collider, the $\bar{p}p$ interaction vertex is Gaussian like distributed along the beamline with $\sigma = 30$ cm. Consequently a long vertex detector is required to have any reasonable acceptance. Long strips can impose a burden on the readout electronics due to increased input capacitance and leakage current. The SVX active region is 51 cm long and consists of two independent cylindrical modules of equal length. A gap of 2.15 cm exists at the center of the detector. The acceptance is ≈ 60 % of the $\bar{p}p$ collision vertices.

The SVX consists of four concentric cylindrical layers (numbered 0–3 in increasing radius). The inner and outer layers are at radii of 3.005 cm and 7.866 cm respectively. The

Number of layers:	4
Inner/Outer radii:	3.005 cm/7.866 cm
Strip Pitch:	60 μm layers 0–2, 55 μm layer 3
Active Length:	51 cm (2×25.5 cm with a 2.15 cm gap)
Resolution:	asymptotic impact parameter $\approx$ 10 μm
Technology:	single sided DC coupled silicon microstrips
Front end readout:	SVX Revision D IC with sparse scan
Signal to noise ratio:	9–10 for normal incidence, most probable MIP
Number of channels:	46080
Number of chips:	360
Power dissipation:	$\approx$ 175 mW/chip
Total power:	$\approx$ 100 watts (includes drivers, regulators)
Cooling:	chilled water ($14°C$)
Beam collision period:	3.5 μs
Support materials:	rohacell, beryllium, alumina, aluminium nitride
Segmentation:	projective wedge (30° azimuth) = 1 readout unit.
DAQ system:	RABBIT + FASTBUS
Readout time:	1–2 ms
Typical occupancy:	7%
Radiation exposure:	15–20 KRad over lifetime

Table 2: Basic Parameters of the CDF Silicon Vertex Detector

location of the inner layer is set by a combination of the readout electronics segmentation and pitch, and the minimum beampipe radius acceptable to the accelerator group at Fermilab.

The amount of material in the SVX has been minimized. This is because the creation of secondary particles and conversion pairs in SVX will be a source of background for all CDF detectors and triggers. In addition multiple scattering will be the limiting factor in measuring the impact parameter of low momentum tracks. And finally the presence of material in the path of electrons from the decay of W bosons will be a source of systematic uncertainty in the determination of the W mass which is an important experimental goal of CDF as well.

2.2 Silicon Detectors

In recent years AC coupled silicon microstrip detectors have become the favored technology for vertex detectors. However, at the time the technology choice was made for the SVX the AC coupled detectors were judged as still too developmental. Consequently an emphasis was put on having high quality single sided DC coupled detectors in a four inch technology and readout electronics which would be relatively immune to strip to strip leakage variations

2.3 Front End Electronics

The front end electronics process signals coming from the silicon strips and communicate with the data acquisition electronics located external to the collision region. The front end system must operate within the timing requirements set by the Tevatron Collider. It must

keep all sources of noise within specified levels and handle loads due to detector capacitance and leakage current. Power dissipation in the front end should be minimized. The front end system consists of a readout chip bonded directly to the strips, mounting hybrids, interface circuits to drive and receive signals, regulate power, and provide calibration pulses and low mass interconnections between detector modules.

2.4 Cooling

Heat generated by the SVX readout electronics, and also due to surrounding detectors, may lead to relative motions of detector components, mechanical instability, damaging stresses, excessive leakage current, and failure of electrical components. For these reasons a cooling system is required which can remove $\approx$ 100 Watts while maintaining an operating temperature close to that present during construction, $\approx$ 20 °C. A further requirement is that the cooling system not contribute excessive mass. With local sources of heat, liquid cooling is the natural choice. The SVX is cooled primarily by flowing chilled water under the readout chips in thin aluminum pipes.

2.5 Data Acquisition System

The DAQ system is required to integrate into the existing hardware, software, and maintenance structure of CDF. It has to contain sufficient parallelism and bandwidth not to introduce any additional deadtime in the CDF readout. Finally it has to provide the required timing and control signals and diagnostic capabilities needed by the front end readout chips.

2.6 Power Supplies and Interlocks

The SVX detector requires power supplies to provide detector bias and operating voltages and currents for the front end chips and interfacing electronics. Due to the remote location of the detector, the power supplies have to protect the system from a range of possible failures and provide fast trip capability with latching of trip conditions. The supplies need to be remotely controlled and monitored. Finally, the power supplies, cooling system, and temperature monitors need to be integrated into an overall interlock system.

2.7 Construction and Testing

In the construction of the detector the scale of the mechanical tolerances must be comparable to the intrinsic position resolution of the strip detectors. In this case the position resolution should be $\approx$ 10 μm using charge sharing information on neighboring strips. In order to achieve position information with similar resolution in the completed SVX detector, the construction errors must then be on order 10 μm or less. This requires care in the choice of materials and assembly techniques and extensive survey during construction and installation.

Since the installed device will be difficult to access during the experiment the electrical systems internal to the barrel must be very reliable. Furthermore to ensure good data quality all components must be tested and characterized before assembly.

2.8 Radiation Monitoring

The SVX detector was conceived to operate during a period when the Collider delivered luminosity would approach 30 pb^{-1}. Studies of radiation levels in the Tevatron Collider indicated that the expected dose would be ≈ 400 $Rads/pb^{-1}$. The electronics and detectors should tolerate this dose with acceptable degradation. Furthermore, it was recognized that the additional dose due to accidents in collider operation, $\bar{p}p$ injection, and studies could be reduced through the use of a system of monitors placed around the collision region and a dose driven abort system for the beams. Such a monitoring system is a valuable tuning aid for the accelerator operators.

2.9 Calibration

Online calibrations of the detector include measurements of pedestals, gains, noise, and other electrical parameters. Due to the large channel count such procedures can generate large amounts of data which can be difficult to filter and evaluate. Specific procedures and analysis tools are required to readily monitor detector performance and provide constants and correction factors for offline analysis.

2.10 Offline Analysis

Reconstruction code for data generated by the SVX must integrate into the existing CDF framework. Specifically, SVX tracking has to link with the CTC reconstruction and provide a capability for refit with SVX hits added to tracks. In addition, new tools are required for vertexing and beamline determination. Finally an alignment procedure using tracks is required to compare with and improve optical alignment constants from construction and survey.

3 Mechanical Design

3.1 Configuration

The SVX overall layout is shown in Figure 2. The SVX is located with its center on the nominal CDF interaction point and consists of two cylindrical modules placed end to end with their axes coincident with the beam axis. Cylindrical coordinates are used here with the z axis parallel to the beamline, the ϕ coordinate giving the azimuth, and the radial coordinate, r, measured along a direction perpendicular to the beamline. The SVX provides track measurements in the $r - \phi$ plane only.

The SVX is mounted inside the Vertex Time Projection Chamber (VTX)[7]. This is a another tracking system which instead measures the event in the $r - Z$ plane. It is used to locate the longitudinal position of the interaction vertex along the beamline and seed the CTC three dimensional reconstruction. While the SVX and VTX have little connection in the offline analysis of track data, they are intimately coupled in an operational sense. Both detectors share the same Argon/Ethane gas volume and cabling flanges. Noise generated in the SVX can affect the VTX. The overall mechanical stability of the SVX relies on the VTX support.

The SVX consists of four radial layers of silicon strip detectors. These detectors are arranged as a twelve sided barrel at each radial position. The detectors are electrically bonded to each other along the beam direction in groups of three. These bonds are made

with 25μm Aluminum wire which is ultrasonically fused to pads on the detector surface. At each radius and on each of twelve faces there are thus a total of six detectors, in two groups of three. These are read out electronically at the two outside ends. Each detector is 8.5 cm long so that an individual readout channel sees a 25.5 cm long strip. The total longitudinal coverage is thus 51 cm. A gap of 2.15 cm exists between the two barrels. The source capacitance of each strip is about 30 pF.

A group of three connected detectors is called a *"ladder"*, and is the basic subdivision of the device (Figure 3). The ladder substrates are fabricated of Rohacell, a light weight foam, and reinforced with carbon fiber strips. Each ladder is individually assembled and mounted. There are four sizes of ladders corresponding to the four radial layers. The total number of ladders is 12 faces x 4 layers x 2 ends = 96, or 24 of each size. In its position on the face of the barrels, each ladder is rotated by 3 degrees about its major axis to allow some overlap between adjacent faces. However, on the innermost layer no such overlap exists. At the outside end of each ladder sits a small circuit board. This circuit is the readout hybrid for the ladder. It contains the readout chips (Section 5.1) for that ladder as well as auxiliary components and buswork needed for the operation of the chips. A photograph is shown in Figure 4. These boards are fabricated using a multilayer thick film process on 0.015 in. thick Aluminium Nitride (AlN)[8]. The readout hybrid also receives cables going to other layers carrying various bussed signals. These cables, fabricated as Kapton flexible circuits, are removable in the case of repair. The hybrid is thermally isolated from the silicon detector to prevent conduction of heat generated by the readout electronics into the detector. A second *"dummy"* board, sits at the opposite end of the ladder for mechanical connection to the support structure (described below). Both the readout hybrid and the dummy board are laser cut and contain a precision mounting hole to allow for the alignment of ladders with respect to a support structure. A group of four ladders at fixed azimuth projects back to the interaction point. This unit is called a *"wedge"*.

The SVX ladders are installed between two support pieces known as *"bulkheads"* using a small screw, O-ring and tapped pin combination which fits through the mounting holes of the ears and attaches to slots machined into the ledges of the bulkheads. The slots in the bulkhead allow the ladder to expand thermally along its length while maintaining good azimuthal location. These bulkheads were made from beryllium to reduce their contribution to the total radiation lengths for the completed SVX detector. Besides being low mass, the bulkheads have been machined very accurately [9] and typically the four circles on which the ladders are mounted have been made concentric to within 15 μm. A photograph of one bulkhead, including cooling pipes, is shown in Figure 5.

In the complete device, an external conductive cylindrical skin surrounds each barrel to isolate it from E.M. noise, external HV breakdown, and to add rigidity to the system. This shield also protects external detectors from noise which may be generated by switching within the SVX. The skin is fabricated as a sandwich of two layers of 50μm Aluminium separated by 1.5 mm of Rohacell foam. Details of the detector geometry are given in Table 3.

3.2 Material Budget

A detailed material budget of the SVX was tabulated during design and construction. A breakdown is given in Table 4. Note that many of the items are further defined in later sections. After completion, the detector assembly was weighed and good agreement was found with calculations. Furthermore, this accounting is used as input to software which

Table 3: SVX Geometry

a: Barrel geometrical parameters

	Radius [cm]	Length [cm]
Layer 0	3.005	25.6
Layer 1	4.256	25.6
Layer 2	5.687	25.6
Layer 3	7.866	25.6

b: Silicon crystal geometrical dimensions

	Width [μm]	$\pm$	Length [μm]	$\pm$	Thickness [μm]	$\pm$
Layer 0	16040	50	85000	50	300	15
Layer 1	23720	50	85000	50	300	15
Layer 2	31400	50	85000	50	300	15
Layer 3	42930	50	85000	50	300	15

c: Characteristics of the active area of the detectors

	Width [μm]	Pitch [μm]	Readout strips	Number of chips	Length [μm]
Layer 0	15360	60	256	2	84500
Layer 1	23040	60	384	3	84500
Layer 2	30720	60	512	4	84500
Layer 3	42240	55	768	6	84500

d: Coverage in polar angle

	Theta $\pm$	Eta $\pm$
Layer 0	6.3	2.9
Layer 1	9.5	2.5
Layer 2	12.6	2.2
Layer 3	17.2	1.9

returns the number of radiation lengths traversed by any track passing through the SVX given its trajectory. Such a code is useful for estimating conversion rates and radiative effects on electrons from W decay. The module is also used in Monte Carlo simulations of CDF. In Figure 6 we present calculated material thicknesses for the total SVX system alone (including cabling) and for the total SVX+VTX+CTC inner support structure. Also shown is the effect of smearing the Tevatron beam spot with a σ of 30 cm. One method to check the effect SVX material is to plot the radius of origin for conversion electrons. These conversions are identified by an algorithm which searches for tracks near an electron candidate reconstructing with the electron to a small invariant mass. In Figure 7 we show this distribution. As indicated, the geometrical boundries of the SVX are visible but the total rate is comparable to other sources.

Material	L0	L1	L2	L3	SUM	x12	
Silicon	2.9	4.2	5.6	7.7	20.4	244.7	
Support	2.2	2.9	3.2	3.3	11.6	139.7	
Hybrids,glue etc.	2.0	2.6	3.4	4.9	12.9	155.3	
Subtotal	7.1	9.7	12.2	15.9	44.9	538.3	538.3
External Screen							53.9
Internal Screen						?	?
Port Card					8.7	104.0	
Clamps and Bus					2.3	27.8	
External Cables					10.1	121.2	
External Tubes						29.0	
Heat Exchanger						30.5	
Gas Manifold						?	
Water						40.0	
Subtotal						352.5	352.5
Bulkhead	R/O	Dum					
Beryllium	40.7	25.6					
Al Tubes	17.8						
Al Port	11.6						
Other	6.0						
Glue	8.5						
Subtotal	84.6	25.6					110.2
Grand Total							1054.9
Measured							1017.0

Table 4: Accounting for material in the SVX construction (in grams). Items listed as ? are not well known but are all very small (few gram range).

3.3 Expected Performance

Given the strip geometry, positions of detector planes, material distributions in the SVX, and the parameters of the CDF magnetic spectrometer an ideal expected performance may be inferred. In the actual device the performance will be degraded by misalignment, mis-

calibration, dead regions, and noise. Based upon Monte Carlo studies and calculations, a set of performance baselines have been determined for the SVX. In Figure 8 we show the track acceptance as a function of track rapidity. The effect of the extended luminous region is clear. In Figure 9 we show the track impact parameter resolution versus transverse momentum. The asymptotic impact parameter resolution is 8 μm. Due to multiple scattering it drops to 53 μm at 1 GeV/c. For tracks which originate at the primary interaction vertex, it is possible to perform a vertex constrained fit using the CTC alone. However for a track coming from a secondary vertex the SVX can be used to improve the momentum resolution. This is indicated in Figure 10.

4 Silicon Detectors

4.1 Detector Design

The silicon detectors used in the ladder construction are DC coupled and single sided. They were manufactured by Micron Semiconductor Ltd[10]. For layers 0, 1 and 2 the strips are on a 60 μm pitch. For layer 3 they are on a 55 μm pitch. The processing steps used in fabrication were optimized for low surface leakage current. In particular, a final sintering step at 400°C in forming gas served to lower the average strip leakage to 300–500 pA for an 8.5 cm strip at 20°C. Consequently the full leakage for a ladder strip was less than 2 nA before irradiation. The detectors all have fully enclosing guard rings which were always grounded through the preamplifier ground on the readout chip. Typical guard ring currents are significantly higher than single strip currents, in the few hundred nA range. It is important that the total detector current (including the guard ring) not be too high because shot noise can cause large fluctuating voltage drops across a 10 $k\Omega$ filtering resistor which is in the bias line. The drops will cause charge to be injected into the readout chip through the detector capacitance which will appear as common mode noise on all read out channels connected to that detector.

4.2 Quality Control

All strips on all silicon detectors used in the SVX were probed both at the manufacturer and at Fermilab during construction. Leakage currents and interstrip resistances were measured. An acceptance specification was applied to the silicon detectors based upon these measurements. A basic principle of this specification was to limit the number of strips with current above 70 nA. These are useless and had to be skipped during wirebonding. Figure 11a shows the distribution of leakage currents for all the probed strips on Layer 2 detectors. Figure 11b shows those which were used in the SVX only. The distributions for the other layers are similar. The strip to strip leakage on a typical good detector is shown in Figure 12.

5 Front End Electronics

A group of four radial layers subtending 15° of azimuth form a wedge of the SVX detector and are an independent readout unit. The full detector consists of 24 wedges. Each wedge contains 1920 silicon microstrips. The overall electrical layout of a wedge is shown in Figure 13. The front end readout circuit is the SVX chip Revision D [11],[12]. There are 2,3,4, and 6 of these per layer respectively. The chips are mounted on readout hybrids and

Table 5: Basic operating parameters of the SVX readout chip, Revision D

Technology:	3 μm rad–soft CMOS
Dimensions:	$\approx$ 6.9 mm square
Number of channels/chip	128
Power dissipation	175 mW/chip
Gain of analog channel	15 mV/fC
Open loop gain	$\approx$ 2000
Nominal feedback capacitor	0.3 pF
Nominal value of charge injection capacitor	0.03 pF
Range of front end (approx)	10 MIP
Leakage current (3 Si detectors (pre–rad))	3 nA/strip
Equivalent input noise (30 pF, quad sample)	2200–2400 e^-
Risetime at sample and hold capacitor	900 ns (10%–90%)
Reset time of charge integrator	700 ns
Maximum digital readout speed	10 MHz
Risetime of analog output	(exponential τ) = 800 ns
Analog supply voltage	6 VDC
Digital supply voltage	5 VDC
Digital data bits	6 chip ID + 2 mode; 7 chan addr + 1 mode

the four layers are bussed up to an interface hybrid called the *"Port Card"*. Finally signals going into the port card are carried through the SVX barrel and out of the VTX on low mass etched copper on kapton cables.

In this section we detail the elements of the front end system.

5.1 The SVX Readout Integrated Circuit

The SVX chip is a mixed analog and digital signal processing circuit. Revision D (SVXD), which is used in the final SVX system, was fabricated in 3 μm CMOS technology. The CMOS process used was not radiation hard[13].

A block diagram of the SVXD chip and timing pattern is shown in Figure 14 and Figure 15. The chip contains 128 identical channels of charge integration, voltage amplification, sample and hold, and comparator/latch. These are followed by a priority encoding circuit which allows a multiplexed analog readout to select only those channels for which the latch is set (or not set). This selective readout mode is called "sparse". Optionally, a global latch line may be asserted forcing a readout of all channels. This mode of readout is called "latch all". When the chip is read out, the address of the channel currently being read appears on a 7 bit address bus along with the corresponding analog level. The characteristics of the the SVXD readout chip are summarized in Table 5.

The SVXD chip was designed to read out DC coupled silicon detectors. In order to have an unbiased threshold comparison on a channel by channel basis it is necessary to subtract the baseline shift due to varying strip to strip leakage current which will be integrated during the sampling time. This process is accomplished in the SVXD chip through a quadruple sample and hold process. In this process, the charge is integrated twice (once "on beam"

and once "off beam"). The results of these two integrations are subtracted. If any particles had passed through the detector "on beam" an excess would remain at the nearest strip.

In a charge integration and sample and hold circuit one integration from time t_1 to time t_2 would use two samples in order to cancel offsets due to pileup and internal charge injections. This is a double sample and hold measurement. The leakage current subtraction described here requires two integrations and is consequently a quadruple sample and hold measurement.

When the analog system noise is measured, a double sample and hold will increase the intrinsic preamplifier noise by a factor of $\sqrt{2}$ for frequencies which are short compared to the inverse of the integration time. A quadruple sample and hole will contribute another factor of $\sqrt{2}$ to double the intrinsic noise. In Figure 16, we show the equivalent input noise (output noise voltage converted to input charge) of the SVXD chip as a function of detector capacitance for both a double and quadruple sample and hold measurement. The fully bonded SVX ladders correspond to about 30 pF of detector capacitance.

The behaviour of the comparator circuit in the SVX chip which controls the sparse readout will be affected by the electronic noise. Rather than having a perfectly sharp transition at threshold, the transition will be spread. The threshold value and its width can be measured by performing a quadruple sample and hold integration and observing the fraction of time a particular channel appears in the readout as the test input charge is varied for one of the two integration periods. A typical channel response is shown in Figure 17. It is possible to unfold the width of the underlying gaussian noise distribution from this curve by a method discussed in Section 10.2.3. For good channels this quantity is 0.4–0.5 fC which corresponds to the quadruple noise shown in Figure 16.

The absolute value of the threshold itself is a quantity which will be affected by chip to chip variations in internal offsets, errors in the leakage current subtraction due to timing and preamplifier saturation, and parasitic charge injection related to the layout of the electrical system on the SVX. The requirement for efficient operation of the detector is to keep these variations at the same level as the threshold width. This is discussed further in Section 10.2.3.

One subtlety of the threshold comparison using a quadruple sample and hold procedure concerns the relative duration of the two integration periods needed to measure the leakage current off and on beam. The sample and hold capacitors which store the integrated leakage current are labeled C_s and C_c in Figure 14. During the first leakage current measurement both capacitors are a load on the output of the inverter labeled $Comp1$. During the second integration the switch R_c is open and the load is only due to C_s. Consequently the risetime of $Comp1$ is slightly different in the two cases. To get an optimal subtraction the two integration periods should differ by this risetime difference. We call this requirement the *"ΔT effect"*. In the SVX detector application, the integration period can only be set to the accuracy of the clock generation circuitry. As is discussed in Section 7.3.1, a design feature of the DAQ electronics, which drive the SVXD readout chips, is to allow for sufficient timing variation for an accurate leakage current subtraction. In Section 11.1 we discuss a procedure used during calibration of the full detector to set these timing differences optimally.

5.2 Readout Hybrids

The basic function of the readout hybrids is to distribute power, ground, and signals to the SVXD chips. In addition, they contain bypassing capacitors for the power lines, resistors to set the current in the SVXD chip integrator, and and a filter for the detector bias line.

An electrical schematic is shown in Figure 18.

Corresponding to the ladders there are four versions of the these hybrids [14]. Layers 0, 1, and 2 are fabricated in 0.015 in. AlN (aluminum nitride), while layer 3 is fabricated in 0.025 in. AlN. This unusual type of substrate was chosen for its good thermal conductivity (about 5 times higher than for the more commonly used Al_2O_3). Circuitry is patterned on both sides with through hole connections using a thick film technology. A larger number of layers were printed on the top side (SVXD chip side) and consequently a small bowing of approximately 0.001 in. was measured due to the higher coefficient of thermal expansion of the circuit dielectric layers over the AlN substrate. For layer 3, which has the largest aspect ratio, the thicker substrate material was chosen to limit this bowing.

The AlN technology choice improved the thermal performance of the detector but required a substantial developmental effort because the thick film system available for this material was not mature. The thermal performance of these circuits is further discussed in Section 6.2

5.3 Interface Circuits

Each readout wedge of the SVX is serviced by an interface card which sits at a radius of 8.81 cm, just beyond the outermost tracking layer. This *"Port Card"* is fabricated on 0.025 in. thick Alumina in multilayer thick film process. The layout of this card is considerably more complex than the readout hybrids. It is constructed with seven conducting layers and a total of 35 separate photomasks. Due to this complexity and also uncertainties in the reliability of the AlN thick film process for this large number of layers the choice of the more conventional Alumina technology was made. The discrete components on this card are surface mounted and all integrated circuits are bare die.

A photograph of the port card is shown in Figure 19. All lines coming out of the port card are distributed in parallel to the readout hybrids of the wedge and then to the SVXD chips themselves. The port card contains a number of different circuits.

To provide operating voltages for the SVXD readout chips, a set of low dropout regulators are used. Based upon test measurements, we determined that supplying regulated power nearby the SVXD chips was very effective in minimizing noise in the system and controlling systematic variations in the behavior of thresholds and offsets chip to chip. The SVXD chip requires two voltages to operate. One supplies the preamp only. The rest of the chip is supplied by the other. A serious failure mode occurs if the preamp voltage is less than the other. To prevent this a diode is placed between the regulators on the port card.

All the digital signals used to control the SVXD chips are received differentially by the port card and then converted to CMOS 5 VDC levels before leaving for the readout hybrids. The SVXD chips have digital I/O pads which are bi–directional. The digital data output by the chip (channel addresses etc.) are converted to differential signals on the port card for transmission to the external DAQ system. The driver/receiver chip set used conformed to IEEE standards RS–422 and RS–485. To minimize power dissipated on the card we chose to back terminate all the differential pairs serially. In this way standing current on the card was reduced significantly.

Analog data generated by the SVXD chips is converted to differential voltages on the port card before transmission to the external DAQ system. These lines are also series back terminated.

In order for the SVXD chip to sparsify the sampled detector signals, a threshold signal is required. This is a voltage step which is input to the preamps through an on–chip calibration

capacitor, one per channel, of 60 fF. There is one calibration input on an SVXD chip. It was not practical to provide calibration lines for each chip however. The choice was made to supply, on the port card, two identical calibration circuits. One provides the voltage step for the innermost layer while the other serves the outer three layers. Radiation effects will be largest on the inner layer. The ability to set a single threshold for multiple layers and still have good efficiency for hits from tracks is clearly a critical requirement for such a restricted system. In fact this worked well as is described in Section 11.1. The threshold voltages are generated by DAC's in the DAQ crates and transmitted differentially to the port cards. The calibration circuits receive, filter, and chop these levels before passing them to the readout hybrids.

A total of 49 lines enter each port card on low mass etched copper on kapton cables. These cables meet a set of larger gauge commercial cables at the outer radius of the VTX chamber and yet another even larger set after leaving the detector gas volume. For the digital lines the cable impedance is 95 ohms. The etched copper on kapton cable which carries digital data was designed to match this impedance as well.

The total power dissipation of the port card is 1.8 watts. Chips on the port card are placed in proximity to the cooling loop on the bulkheads in proportion to their power dissipation.

5.4 Interconnects

The readout cable (known as a *"pigtail"*) attached to the end of the readout hybrid incorporates a *"gold-dot technology"* [15] to make electrical contact to a mating bus cable which serves each wedge and connects to the port card. In this technology, small gold plated bumps are deposited on traces at the end of the flexible Kapton pigtail cable. These bumps mate with the bus cable, which contains pads of a similar size, using a lightweight G–10 clamp fastened with a small bolt and nut to provide the necessary mechanical pressure to ensure electrical contact. The interconnect pitch used has traces on staggered 40 mil centers, giving an effective 0.020 in. pitch. This connection scheme has many advantages. Contact can be broken and re–established an arbitrary number of times. This allowed easy testing of ears and ladders before final assembly into the barrels. The mass of the interconnect is minimized. It also allows considerable flexibility of layout and spacing of traces. Conventional mechanical connectors are only available for traces on 0.050 in. pitch or larger and occupy excessive space. The gold dot scheme is illustrated in Figure 20. The layout of the busing cables and the clamps can also be seen in Figure 21.

No failure of a gold dot connection occurred in the SVX to date.

6 Cooling System

6.1 Specification and Design

Approximately 50 Watts are dissipated by the SVXD chips and the port cards located inside each SVX barrel. This power can change by 5–7% depending upon the operating mode of the front end chips. In addition, the ambient environment of the SVX is heated to about 35^0C by the surrounding CDF detector components. Without external cooling, the SVX barrels would rise to a temperature of about 90°C in approximately 20 minutes. To avoid relative thermal motions of detector components, mechanical instability, damaging stresses, excessive leakage current, and failure of electrical components, a cooling system is required

which can remove the heat load while maintaining an operating temperature close to that of construction $\approx$ 20°C. In addition, the elements of the cooling system on the SVX barrel should be as low in mass as possible. With the sources of heat being rather localized, liquid cooling is a natural choice.

A thermal model of the readout hybrid and bulkhead system is shown in Figure 22. The desire to keep material as far out from the interaction region as possible led to the design shown wherein heat is conducted partially along the length of the ceramic. Calculations and measurements on models indicate that the temperature drop between the SVXD chip and the cooling water is of order 10°C. The result of one such calculation which compares a number of substrate materials is shown in Figure 23. Measurements also indicated little variation in the behavior of the SVXD chip up to 60°C.

The SVX cooling system is shown in Figure 24. Two Neslab CFT25 chillers deliver chilled deionized and filtered water, one for each SVX barrel. The chillers were originally to be placed far from the SVX barrel and therefore we have a bypass loop to return most of the water directly to the chiller. Approximately 10 gr per second of water is sent to each barrel. The chiller runs at 13°C. The water just before reaching the SVX is about 19°C. The SVX bulkhead temperature during normal operation is $\approx$ 25 °C. The chilled water circulates through thin 3003 series $\frac{3}{32}$ in. outside diameter aluminum tubing, with 0.014 in. wall thickness, which is formed to the shape of the bulkhead and glued to the bulkheads just below the SVXD chips on all four layers. After testing many epoxys we chose to use Master Bond brand EP21ANHT thermal epoxy because it was sufficiently strong and had very good thermal properties. The two input and two output cooling tubes for each SVX barrel are glued to the outer SVX screen with the same epoxy. This provides additional cooling and acts to thermally isolate the SVX from its surroundings. The entire cooling circuit is kept under negative pressure. The pressure drop through the circuit is about 7 PSI. The lowest point on the circuit is kept about 3 PSI so that the pump in the chiller does not cavitate.

The number of readout chips varies from 2 to 6 per ladder for the 4 layers of silicon and the typical heat load is 175 mW/chip, giving a total heat load from the readout chips of 31.5 watts per barrel. An additional cooling circuit is used to remove heat from the port card, which due to its power regulating and signal driving functions, generates 1800 mW each or 21.6 watts per barrel. Thus, a total of 53.1 watts of heat is typically generated by the electronics in each half of the SVX.

A system to flow chilled gas through the SVX barrel was also constructed in an attempt to even out the temperature distribution and provide slightly more cooling capabilities. A cast aluminium tube with a fin–shaped outer diameter acts as a heat exchanger. The input chilled water flows through it, and the gas to be cooled flows between the aluminium fins and a shrink–tube enclosure. The entire heat exchanger is 34 cm long. The temperature of the SVX is monitored by 12 AD592CN temperature probes per barrel, located throughout the device. The chilled gas system is observed to have a very small effect on the overall temperature distribution of the SVX.

6.2 Performance and Operating Experience

The cooling system operated almost continuously for about one year with few problems. The flow rate at a given pressure drop through the system was still approximately 90% of its original value at the end of the run, indicating that there was little or no flow restriction in the aluminium tubing.

According to the temperature sensors located throughout the detector all monitored locations were within 3°C. The largest temperature drop was between the bulkhead which averaged 22°C and the silicon closest to the port card which was typically 25°C.

A number of measurements were performed during commissioning which determined various thermal time constants of the system. The time to cool or warm up the the entire SVX was determined by the capacity of the chiller. We observed that for a given set of wedges under power and the chiller at fixed temperature, the addition of another wedge raised the bulkhead temperature by 1.2°C near the wedge with a time constant of about 110 seconds. If cooling water is abruptly stopped and then restarted the recovery time constant is about 60 seconds if the water is still cold. For single wedges under power strong correlations were observed for temperature probes near the wedge. To prevent possible mechanical distortions, we avoided situations where, for example, half the wedges were powered all on one side of a barrel.

7 Data Acquisition System

7.1 System Architecture

The architecture of the SVX data acquisition system was determined by the SVX detector design, the operation of the SVXD chips and their need for a variety of clocking sequences, the required readout speed, and the existing CDF data acquisition network [16]. The system consists of a FASTBUS Sequencer, a Crate Controller, and a set of Digitizer modules. Additional details can also be found in the literature [17],[18],[19]. The CDF SVX detector was instrumented with four Fastbus crates and four SVX RABBIT [20] crates each with 6 Digitizers to accommodate 24 SVX wedges as illustrated in Figure 25. All SVX Fastbus crates are connected to a single cable segment in a Fanout crate.

The standard interface to the CDF data acquisition system is provided by a SLAC Scanner Processor (SSP)[21], a commercial product that is used extensively in the CDF network. It is a programmable Fastbus master that can reformat the event data and attach header information. It has adequate memory to buffer four events, a feature used in certain calibration modes.

The Sequencer, a FASTBUS slave, is based partially on the SRS CAMAC module cited in Section 10.2 [22], but incorporates many additional capabilities. It is a programmable module which provides the clocking signals necessary to operate the SVXD chips, synchronization logic to link to the CDF data acquisition system, and contains storage for one event as a pipeline to the SSP.

The Controllers and Digitizers are housed in SVX Rabbit crates on the CDF Central Detector. The Controller provides the interface between the Digitizers and the Sequencer. The Digitizers process analog data and buffer digital data from the wedges. They are read out by the Controller.

7.2 Control and Data Flow

The Sequencer can read from and write to both the Digitizers and the Controller. It is also possible to direct the read information out a front panel port on the Digitizers to operate with a standalone online monitoring system. The primary mode for reading out wedge data is via automatic scans in which the Controller reads the wedge data register in each of its Digitizers reporting the presence of data.

Twelve signals control sample and hold operations within the amplifiers as well as the event readout. During beam crossings, the SVX timing signals pass from the Sequencer through the Controller and Digitizer to the wedge. Sample and hold operation is synchronized with the 3.5 μs beam crossing interval. During readout, the timing signal drivers turn off, and the digitizer accepts the chip and channel addresses along with the analog data from the wedge. The Sequencer also issues a convert signal telling the ADC on the Digitizers when to begin the hold and digitize cycle. Once the data for a channel have been prepared by the Digitizers, readout can commence. The Controller is commanded by the Sequencer to initiate a scan read. In this mode the controller will poll each digitizer and only send data to the Sequencer for those Digitizers which have responded that they have data. The SVX IC's will normally be programmed to provide sparsified data which will cause the Digitizers to stop responding as each wedge becomes empty. The Sequencer monitors the presence of data in the wedges and terminates the readout after all the wedges have been emptied. A 32 bit Read–Data path from the Digitizer to the Sequencer carries data during a read or presents data status from each Digitizer when a read is not in progress. Both the data and their status can be masked off. The data from any wedge can be masked in the Controller and data status is maskable in the Sequencer.

A compact data format was used to describe the digital and digitized analog output from the SVXD chip. Each hit is described by one 32–bit word. The control registers are read from the Digitizer or Controller modules using the same format as for the hit information. Data from all the Digitizer and Controller registers are read out with every event and appended to the raw data for diagnostics and calibration purposes.

The algorithms for the readout of the SVX Sequencer include data acquisition and data calibration modes. During data acquisition and data mode calibration (every event is read out to a disk), the SSPs read data from each Sequencer's buffers until an end of block code is returned. Then a check is made between the number of data words transferred and the actual number of words written to the Sequencer's block. In case of a mismatch, an error condition is reported to the system. The raw data words are then sent through the DAQ chain and are written to disk. In scanner mode calibration the raw data words from the Sequencers are sent only to the SSPs. For each channel, the scanner accumulates the sums of relevant quantities as well as the number of events read. After collection of the predefined number of triggers, the data accumulated by the SSP are sent the rest of the way up the DAQ chain to be further analyzed by calibration consumer processes. This method of calibration runs much faster than in the data mode because it reduces the number of data transfers and uses the computing power of the SSP.

7.3 System Modules

7.3.1 The Sequencer

The block diagram of the Sequencer is shown in Figure 26. One Sequencer can control and readout up to eight wedges of the detector. The Sequencer consists of a microsequencer chip, a program memory array and pipeline register and produces the clock patterns required to operate the SVX IC. The Event Memory and End of Buffer and Memory Management logic provide for temporary storage of the data for one event. The Event Memory is separated into eight 2K buffers each holding the data from a specific wedge. All registers and memories are accessible through Fastbus.

The IDT 49C410A [23] microsequencer contains a 16 bit program counter, 33 word

Microprogram Control	Crate Control	SVX Pattern Control
Micro Instr (3:0)	Sub Adr (3:0)	Vernier Ctrl (3:0)
Done	Slot (3:0)	NIM output (3:0)
XQT Hold	Function(2:0)	Vernier Adjustable:
Seq Function(2:0)	Test (3:0)	NIM output (3:0)
Branch Ctrl (6:0)	Data (15:0)	Digitizer (5:0)
Branch Adr (15:0)	XQT	Pattern (11:0)

Table 6: Bit assignments for the SVX Sequencer

deep stack and register that can be used for loop control. External logic provides for 32 branch conditions in their true and complement form as well as an unconditional branch. Instructions from the 16K word by 96 bit program memory are executed in the pipeline register. This 96 bit register can be thought of as a set of fields that describe functions to be performed during the present instruction execution as illustrated in Table 6. The Microprogram Control determines how the microsequencer generates the address of the next instruction. This address is used to point to the program memory location of the next instruction to be executed. That instruction is loaded into the pipeline register to begin the cycle again. The Crate Control allows read/write access to any register in the SVX Rabbit Crates, and the SVX Pattern Control governs the timing transitions for the SVX IC. In this way transitions on control lines can occur as often as each instruction is executed.

The Sequencer provides the timing signals necessary to operate the SVX IC and these signals must be synchronous with the beam crossing. Additionally, these signals must be tailored to the requirements for each phase of sampling and acquiring/rejecting an event as well as calibration and monitoring of the detector. The clock frequency for the microprogram engine is 12.5 MHz. The timing signals that operate the SVX IC are controlled directly by the program running. To eliminate timing jitter associated with the sequencer clock, the clock must be synchronized with every beam crossing.

To accomplish this, the Sequencer's clock is started by an external signal that is related to the beam crossing, and it is stopped before the next beam crossing signal. During the time when the sequencer's clock is operating, the internal program is generating the SVX IC timing pattern appropriate for sampling an event. The Sequencer program will execute 43 instructions during the 3.5 μs interval between beam crossings, which includes the overhead of stopping and restarting the clock.

It is necessary to control the widths of some of the timing pattern lines to within 10 ns over a period of 1μs. This is due to the ΔT effect discussed in Section 5.1. Since the edges of these lines are determined by the 80 ns clock period a method for delaying its arrival was developed and is illustrated in Figure 27. The SVX Pattern Control field of the instruction controls a delay line circuit that produces clocks for the pattern portion of the pipeline register. A three bit field of the instruction selects one of 8 possible delay taps for use in clocking the SVX Pattern.

7.3.2 The Controller

The Controller interfaces the Sequencer to an SVX Rabbit Crate. A block diagram of the Controller is shown in Figure 28. It provides read and write access to all registers in the crate and passes the timing signals for the detector from the Sequencer to the Digitizers. The function code, slot, and subaddress information from the Sequencer are used to direct single word read and write operations as well as multi–word readout scans and broadcast operations. Digitizer data as well as status indicating the presence of data are issued to the Sequencer upon request. The front panel has five high density 36–pin connectors, three for receiving and another two for sending. Information from the SVX Timing Cable is passed directly to the Rabbit backplane.

The Controller translates function codes from the Sequencer. In a write operation to the Digitizers, control information along with the Write–Data from the Sequencer is driven onto the SVX Rabbit backplane. The appropriate addressing and control lines are set to cause the specified register on the addressed Digitizer to accept the data. In a read operation, the Read–Data cable will be driven by the Controller along with a signal to tell the Sequencer that the data is valid. Data can come from either the Digitizers or from internal Controller Registers. It is also possible to direct the read information to a front panel port on the Digitizers. In addition to single word operations, the Controller can be commanded to scan the data from an entire crate eliminating the need to directly address a Digitizer for each word of data; a crate scan pushes data at a rate of 12.5 MHz.

7.3.3 The Digitizer

The Digitizer passes the clocking signals from the Sequencer to the detector and receives digital data and analog signals from the detector wedge. It contains registers for storage of digital data and a section for processing and conversion of the analog data. All of the digital information is formed into a 32 bit word that can be read out by the Controller.

As shown in the block diagram in Figure 29, the Digitizer contains a 12 bit ADC, three 12 bit DACs and registers for data, control and status. The ADC is a Datel 132S, with built in sample and hold, and an overall throughput of 2 MHz. A large offset voltage that accompanies the signals from the detector must be subtracted before any gain adjustment can be applied. One of the three DACs supplies a voltage for this purpose. The programmable gain can be adjusted over a range of 15 equal steps. Each SVX wedge contains 2 calibration pulsers, each controlled by a separate calibration voltage. The pulsers are fired by one of the timing signals supplied by the Sequencer. Two of the three DACs supply these separate calibration voltages.

7.4 Synchronization with the CDF DAQ

The operation of the SVXD chip is performed by an ensemble of timing signals generated by the Sequencer module in phase with the bunch crossing times regardless of the uneven spacing of alternate bunches. For this reason the Sequencer has to be synchronized with every beam crossing. The method also minimizes the impact of the jitter of the Sequencer's internal clock on the precise timing of the event and threshold integration times.

The 53MHz CDF Master Clock generates timing signals correlated with the Tevatron bunch crossing times. Their edges are timed with 1 ns resolution relative to the bunch crossing. The Tevatron operates with 6 bunches alternately spaced by 185 and 186 clock cycles. One of these signals, SVX–Sync, is used by an LRS4222, a programmable delay

module to generate a sequence of the start and stop pulses for the control of the operation of the Sequencer's internal clock. SVX–Sync preceeds the next beam crossing by a fixed time.

The SVX sample and hold cycle contains 43 Sequencer timing cycles. To ensure accurate leakage current cancelation this timing must be stable. The duration of the 43 cycles was measured to be accurate to better than 1 ns.

The CDF data acquisition system is based upon a multi–level trigger which determines readout of the detector [24]. The first level trigger (L1) is determined before the next beam crossing. In the case of a L1 accept deadtime is incurred until a second level (L2) decision is reached. The time for L2 varies but is typically 20–30 μs. In the case of a L2 accept full readout of the detector would commence. The data thus acquired is subject to a further filtering in a third level software trigger before being written to tape. The operation of the SVX Sequencer is linked to the various L1 and L2 decisions.

In Figure 30 an example of the microsequencer program block diagram is presented, performing an event acquisition during the collider run. The program starts with the downloading of the chip numbers to the chips' memories and reading them back for the diagnostic purposes. This part of the program is executed only once. Then the Sequencer's clock is shut off, waiting to be synchronized with the next beam crossing. After receiving the start clock signal, the Partial Reset procedure is executed in which only the chip integrator is reset and the events sampled in the previous crossing are kept on the Sample and Hold capacitor. Then a check is made of the level of the L1 trigger decision signal.

The absence of the L1 trigger signal is an indication to integrate a new sample. When the integration cycle is finished the Sequencer's internal clock is stopped by the next stop clock signal and the synchronization with the next beam crossing takes place. The following start clock signal enables the operation of the internal clock again and the Partial Reset is performed. There are 43 80 ns microsequencer's instructions executed between the Start–Clock and Stop–Clock sequence.

The presence of the L1 trigger signal indicates that the event stored during the previous crossing passed the L1 trigger conditions and the event may be prepared for readout. In this case a threshold sample is taken, which is used to cancel the leakage current component in the event sample. The event sampling and the threshold cycles must be executed with the full knowledge of the beam crossing. In the first case the beam crossing should appear inside the integration window and in the second one the integration must be performed between the beam crossings. The threshold restoring subprocess, shown in Figure 31, requires two beam crossings to be performed with the constraints defined above. The microsequencer program inhibits generation of the Stop–Clock signal at the LRS4222 during the threshold cycle. When the threshold is restored, the synchronization mechanism is enabled again.

In the next step a test is done of the L2 trigger decision. Its presence initiates the readout cycle and its absence directs control to the synchronization subprocess. The Start Scan Latch signal is automatically reset when is it checked by the execution of a conditional branch microsequencer instruction. During the readout cycle the synchronization mechanism is disabled again until the cycle is finished. To indicate that readout is finished, the Sequencer sets a particular bit in one of its CSR space registers. The SSP continually polls this register after sending the Start Scan message and will recognize the signal and begin to read out the Sequencer within 2 μs of the bit being set. For non–triggered events, a separate integration cycle is performed in the very next Start/Stop clock cycle.

7.5 Scan Times

All detector elements in the CDF data acquisition system are required to read out within 2 ms. Due to the large number of channels it was necessary to partition the SVX into four independently read branches. The scan time is defined as a sum of two components: the time required to read SVXD chips in six wedges by the Sequencer and the time to move data from the Sequencer's Event Memory to the SSP's buffer.

The Sequencer scan time is proportional to the number of hits multiplied by the sum of the duration of the basic chip data cycle, called HiLo, the response of the front end modules, signal propagation delays and the time required by the Sequencer to check that all the data are read out from wedges. The Digitizer's data register can be read out in two modes: sequential and pipelined. Only the faster pipelined mode was used in SVX operations. In this mode a HiLo cycle is followed by the crate scan instruction and followed by another HiLo cycle, before the previous scan is completed. The duration of the pipelined readout is determined mainly by the length of the HiLo cycle plus a small overhead associated with checking if the previous scan was finished.

The total length of the HiLo signal was 2.08 μs. It was set to accommodate the chip response time and the risetimes of signals on the cable. The scan times for reading the front end modules by the Sequencer for different number of channels are presented in Table 7 assuming even occupancy across wedges. The difference of the scan times corresponding to the time needed to read out one channel was understood in terms of the 250' cable propagation delays (800 ns), ADC conversion cycle (500 ns), crate readout time (100 ns) and the length of the HiLo cycles. For pipelined readout, the scan times are independent of the number of Digitizers read if the HiLo cycle is longer than the sum of the indicated components.

Table 7: Values of the Sequencer and SSP scan times [ms]

Occupancy	1 Digitizer	6 Digitizer	SSP (6 Digitizers)
10%	0.41	0.41	0.36
20%	0.81	0.81	0.59
40%	1.61	1.61	1.04
100%	4.02	4.02	2.40

The time required to move data to the SSP was measured as a function of occupancy and is illustrated in Table 7. The SSP's overhead associated with establishing a FASTBUS connection between the modules was measured to be 140 μs and the block transfer rate equal to 200 ns per 32 bit word.

The SVXD chip has the ability to sparsify the data and read only channels above the threshold. The number of hits per interaction is a function of the following factors: event multiplicity, noise fluctuations above the threshold settings, uniformity between chips in a wedge, number of low momentum spiral tracks and beam gas interactions. The average occupancy changed with radiation. As discussed above, for pipelined mode the scan time will be determined by the most occupied wedge. A plot of total scan time versus the most occupied wedge is shown in Figure 32. The observed occupancy, its fluctuation, and its effect on scan times, is discussed also in Section 11.1.

7.6 System Microcode Structure

A set of specific programs was generated to perform the event acquisition and calibration tasks. The microprograms were tested on various test structures (ears, ladders and wedges) taking special attention to the optimization of the performance of the detectors. The programs were written in an assembler language designed specially for the application in this system.

7.6.1 Description of the Meta–Assembler

The Sequencer's microsequencer chip executes 96–bit wide instruction words, divided into three parts, that provide pattern timing and data latching signals, crate data and control codes, and microsequencer conditional control logic and branching instructions. The HiLevel Assembly Language Environment[25](HALE), a relocatable macro meta–assembler program, was used to define source program definitions of instruction formats. The design objective was for any user to be able to write a program using only logical mnemonic terms for the desired functions, without having to know anything about the format of the Sequencer control word. The necessary file structures naturally divide into three forms: the definition files, that specify the format of the microcode word and the value of any useful symbols; the source files, that contain the sets of macro calls used to write the actual programs; and the format files, that store the compiled microcode in a format that can be easily downloaded in to the device (in this case, ASCII).

7.6.2 Logical Divisions of the System Code

There were many similarities between the microcode used for data calibration and acquisition operations. Therefore programs were structured into several separate functional units, which were coded and compiled separately using HALE. Typically an individual module would exist to perform an operation such as loading of SVXD chip ID's, integration of charge, or latching of data.

8 Power Supplies

The power requirements for the SVX include multiple low voltage levels to drive electronics on the port card and ears, as well as multiple higher voltage levels to bias and deplete the silicon detectors. Certain critical relationships between these voltages during power–up and operation complicate the overall specification of the supply. The need for remote control and monitoring of the supply complete the basic list of criteria that shaped the design strategy for the SVX Power Supply (SPS). In this section, we discuss in detail the specification, design and performance of the SPS.

8.1 Specification

The design specifications for the supply can be arranged into four groups: basic power requirements, critical voltage relationships, failure mode protection and control and monitoring. We address each of these elements below.

1. Basic power requirements: Table 8 shows the voltage requirements for a wedge during operation. Space restrictions require that the supply be located about 17 m from

Table 8: SPS voltage specifications. The values in parentheses are the nominal voltages at the port card after taking into account lead drops.

Line	Function	Nom. Voltage	Max. Current
AP	Analog Power	+8.0 V (7.4)	0.250 A
DP	Digital Power	+7.0 V (6.4)	0.400 A
Vcc	Port Card Dig.	+5.2 V (5.0)	0.125 A
VP	Pos. Rail V.	+6.0 V (6.0)	0.025 A
VM	Neg. Rail V.	-6.0 V (-6.0)	0.025 A
B0–B3	Bias layer 0–3	0–80V	1 mA

the detector. While the port card electronics were relatively insensitive to supply regulation, the SVXD chips were supplied by regulators located on the port card. These features reduced the need for strict regulation of the supply to easily attained levels, shifting the problem instead to one of optimizing cable diameters. The need for independent control of each wedge suggested using isolated outputs for each wedge in order to reduce both the coupling to external noise sources and the effect of ground loops.

2. Critical voltage relationships: Three critical voltage relationships placed constraints on the SPS design. First, the CMOS design of the SVXD chips demanded that the Analog Power (AP) voltage always remain above the Digital Power (DP) voltage minus a diode drop. Failure to maintain this condition results in an excessive current draw on DP which is sufficient to cause fusing of wire bonds to the chip. Since the detector is non–serviceable during operation, such a loss would be permanent.

   Second, if high bias voltages are applied to the input of the SVXD chip without low voltage power to the chip, large voltages may develop across the gate of the input transistor thereby causing damage to the input. The SPS must prevent this occurrence.

   Third, if low voltage is supplied to the SVXD chips without sufficient voltage on the detector to reverse bias it, (a bias voltage less than about 2.5 V), then the input of the charge integrator is pulled to ground driving the amplifier to the rail. This condition is also undesirable over extended periods of time, and should be avoided as a matter of design.

3. Failure mode protection: Failure mode protection in the specification was intended not only to prevent supply failures from damaging the detector, but also to minimize the possible effect of failures in the detector. The most important failure mode to guard against is a loss of AP voltage without a simultaneous loss of DP. Should such a loss occur, the supply should be designed to prevent wire bond fusing. Double or triple redundancy against failures of most voltage levels was required, again owing to the lack of serviceability of the detector.

   Overcurrent conditions that develop outside the power supply should be interrupted in order to prevent or minimize damage to affected components.

The philosophy adopted for hardware failure mode protection extends as well to operator error and errors in control programming. Sound design requires that the hardware prevent operation of the supply in a mode that could cause damage to the detector through faults of omission or commission by the operator. In substance, this demands that the power–up sequence and the voltage specifications be enforced by hardware.

Finally, failures in one wedge must not affect the operation of any other wedge.

4. Control and monitoring: The voltages for each wedge must be independently controlled. Bias voltages levels must be set independently. All control functions must be performed remotely. Voltages and currents must be remotely monitored in order to watch the operating characteristics of both the supplies and the wedges. The supply must provide a means to establish a complete interlock with external systems, including both an input by which to shut the supply off and an output to report the status of the supply.

8.2 Design

Simplicity and cost were the primary motivating forces behind the design. Given the complexity of the specification, added attention was paid to design simplicity in order to ensure high reliability at low cost. The design solution consists of a single supply for every wedge. Each SPS consists of three sections in a single package: independently controlled bias and low voltage sections, plus a digital interface. The bias section contains four independently controlled, isolated output channels. Voltages on these channels are determined by four internal DAC's set through the digital interface. A single *"bias enable"* line switches the supply outputs between zero and the value stored in the DAC's. Two internal op–amps on each channel provide analog voltage and current monitoring through a rear panel connector. The current monitor is sensitive at the 10–30 nA level.

The low voltage section consists of five fixed–voltage outputs. A single *"low voltage enable"* line switches all low voltage channels between the "on" and "off" states (the "off" voltages are actually above zero, but effectively turn off the detector electronics). Internal op–amps on each channel provide analog voltage and current monitoring. Each low voltage output (except for DP) derives from a LM333 or LM350 regulator driven by a common ± 12 V power supply. The enable line is a feature of these regulators. The driving supply, selected on the basis of low power output and cost, at once provides one level of protection against failures in the downstream regulators, and is itself a highly reliable design. The output of AP drives the DP regulator, thereby providing a complete interlock on the AP and DP voltage levels.

The SPS provides low voltage over–current protection at two levels. First, fuses on each low voltage output is limited by a 1 A fuse (0.5 A for VP and VM). Second, comparators continuously monitor the current on all channels and trip the supply when any current exceeds a specified design limit. Bias lines are current limited.

A series of comparators monitor all output voltages and trip the supply when any deviate from design tolerances. Both upper and lower limits are imposed on AP, DP Vcc and the internal DAC reference voltage. A zener diode to ground after the fuse on the output of Vcc affords additional over–voltage protection for the port card digital components.

Another set of comparators enforces the power–up sequence by inhibiting the LV enable line internally and changing the bias over–voltage limit when the low voltage is off. The entire set of voltage and current limits is listed in Table 9.

Table 9: SPS internal trip specification. OC refers to the current at which over–current trips occur, OV to over–voltage, and UV to under–voltage. Indicated percentages are taken as fractions of nominal.

Line	OC	OV	UV	
DP	0.80 A	+5%	-5%	
AP	0.40 A	+5%	-5%	
Vcc	0.32 A	+5%	-5%	
VP	0.05 A	none	none	
VM	0.05 A	none	none	
DAC +5 ref	none	+5%	-5%	
+12 V	none	none	-5%	
Bias	1 mA	8 V	none	(LV disabled)
Bias	1 mA	80 V	3.0 V	(LV enabled)

Each supply is controlled by 15 TTL input lines plus a single global enable line. All lines, except the global enable, are dedicated to a single supply. The global enable line is daisy–chained across supplies. Both TTL and global enables lines are positive control such that interruptions in controller power or cables disable the supply.

Sixteen TTL and 18 differential analog readback lines allow remote monitoring of supply operation. The TTL lines indicate when a supply has tripped and latch the reason for the trip. A simple logical OR of the trip status line from each supply sufficed as an external status line to trigger hardware for the experiment.

Control and monitoring of the system is established though a set of CAMAC modules with communication via the Fermilab Accelerator Controls Network [26],[27]. This system provided a high level programming environment for control software that rapid implementation of basic controls and monitoring functions in an advanced graphical interface. A block diagram of the SPS system as implemented in CDF is shown in Figure 33.

8.3 Performance

The SPS has met all design objectives. Extensive testing prior to field service showed that the supplies operate in extremely predictable ways during trips, surges or interruptions in line power. Despite the many trip circuits, the SPS is not very sensitive to external sources of noise, a concern raised early in the design phase. Large beam losses into the detectors, however, have initiated over–current trips in the bias lines. Such events were a problem primarily during the early portions of accelerator commissioning. Some existing supplies have been modified to provide up to 5 mA at 45 V, or 2 mA at 80 V with only changes in a few resistance values. We have experienced no supply failures in the field.

9 Interlocks

The internal power supply trip circuits described in the previous section protect the SVX from a range of electrical failures. In addition, the temperature probes on the SVX, along with pressure sensors placed in the chilled water circuit are inputs to an interlock system used to protect the SVX from damage due to overheating or cooling water leaks. The

interlock system is based on a Texas Instruments 405 series programmable logic controller. This device is instructed to turn off all SVX power supplies if monitored temperatures are too high. If the pressure in the chilled water circuit approaches atmospheric, the power supplies and chiller is turned off to avoid damage to CDF due to a water leak. In day–to–day operations, non–experts are in contact with the device. Without the interlock system this would not be possible. This system has proved to be a reliable and inexpensive safety net for the SVX.

10 Construction and Installation

Further details on construction of the SVX can be found in the literature, [28], [29], [30].

10.1 Ladder Mechanical Assembly

The three detectors in a ladder are glued to a lightweight Rohacell [31] and carbon fiber support structure. Figure 3 shows the layout of an SVX ladder. The Rohacell is a polymethacrylimide rigid foam of very low density with good mechanical properties. This foam is first milled to the desired dimensions and then carbon fiber strips are epoxied into it using a compression mold heated to 125°C. These ladder substrates are typically made flat to within 75 μm. During the detector gluing operation, the detectors are placed on top of the ladder substrate and are held in gluing fixture utilizing a vacuum chuck. One such fixture is shown in Figure 34. Since the strips of the three detectors on a ladder are connected electrically, it is necessary that the detectors are aligned to one another to better than their intrinsic position resolution. To accomplish this, the gluing fixture is mounted on a granite table and the detectors are aligned by focussing on the strips with a high–magnification TV camera mounted on the measuring arm of a Coordinate Measuring Machine (CMM) [32] and moving them into position with micrometer adjustable stops. The reference line for the detector alignment is a line, established by the CMM software, through the centers of the laser–drilled mounting holes in the circuit boards at both ends of the ladder. Each of the three detectors are adjusted so that their center strip is aligned to this reference line. The epoxy [33] used to glue the detectors to the ladder substrate exhibits very little shrinkage or outgassing during the low temperature (60°C for two hours) heat curing process. Figure 35 shows that the detector alignment after gluing has an rms of 4.5 μm and is consistent with the 5 μm measurement repeatability calibration of the CMM.

10.2 Ladder Electrical Assembly and Testing

In this section we will discuss the ladder electrical assembly and testing procedures. Many of the electrical tests formed the eventual basis of online calibrations which were used during colliding beam running with the full SVX detector. Naturally they evolved in complexity and precision through that process. The online calibration results are discussed in Section 11.1 but all the formalism and derivations which are relevant are given here as a reference.

Preceding the ladder mechanical assembly described above, the separate electrical units were processed and tested. These steps included detector probing (see Section 4.2), SVXD chip probing, and readout hybrid assembly and test.

All electrical tests on chips, hybrids, and ladders were performed with a set of CAMAC based readout and driving electronics developed for the prototyping of the SVX detector

and SVXD chip. This set consisted of a programmable pattern generator (the SRS) and a flash ADC/memory module (the SDA) [22].

Each wafer, containing 110 SVXD chips, was evaluated using an automatic probe station before dicing. The chips were tested for basic digital function, power supply currents, noise, gain, and analog offset level, sparse readout, and for the presence of dead channels. Although the yield differed from wafer to wafer, typically 50–60 % of the chips were perfect. Notably, on a subsequent production run of the same chip for another customer the yields dropped to 15 % for no identifiable reason.

In the assembly of readout hybrids, the chips attached to the same hybrid were selected in groups that had DC analog levels within 7 mV of each other as determined during wafer probing. After assembly their main electrical features (response to charge injection, stability, chip ID readback, channel addresses, positive sparse, negative sparse) were checked. The standard burn–in was to operate the modules at room temperature under clocking for 100 hours. No modules failed after this burn–in.

After mechanical assembly and survey the ladders were wirebonded, tested, and if necessary bad strips or areas were repaired.

The SVX ladders were wirebonded on a Kulicke and Soffa Model 1470 aluminum wedge bonder with a 30 degree wire feed. Although this machine had an automatic (programmable) bonding capability this was not used. All bonding was done in manual mode.

At the time of installation the SVX detector had 3% dead or noisy channels. To a large extent these could be traced to problems which occurred during the wirebonding process. This was a major quality control factor in the construction of the full detector. Most of problems were due to cases where the bonder either lost the wire, bonded in the wrong place, or struck the oxide between strips. Procedures were developed which allowed certain damaged regions to be substantially recovered. This is discussed in Section 10.2.4 below.

A total of 125 ladders were put on the bonding machine, 108 ended up to be working ladders. The electrical ladder assembly and testing had an overall yield of 86.4%. The losses were due to electrical failures observed after wirebonding (8.8%), accidents during which ladders were damaged or broken (3.2%), and situations where the wirebonding failed to work (1.6%).

The ladder testing procedure involved quantitative measurements of response, noise, and sparse threshold. The data collected was used to select good ladders and sort ladders into wedges with similar electrical properties. Using this data, bad regions were scattered around the detector to maximize the acceptance. In sections below the specific measurements are discussed. These measurements also form the basis of calibration procedures which were carried out during online operation of the detector for physics.

During testing, dry air was always circulated inside the testing chamber. This was necessary in order to obtain consistent measurements of the detector properties. In particular, a subset of the ladders showed particular sensitivity to moisture. These ladders would have large leakage currents, especially near the edges, which persisted for up to one hour in a dry atmosphere. After that drying out period they behaved more like typical good ladders. Because of this easy improvement we never used this moisture sensitivity as a criteria for rejecting a ladder. Later during operation of the SVX detector in the Collider, most of these ladders showed anomalous surface currents again. This effect, which in the end was more annoying than significant in terms of the successful operation of the detector, will be discussed in Section 13.3 below.

10.2.1 Gain and Offset Measurements

The measurements of gain and offset are a basic quality test of the analog signal coming out of the SVXD chips. Figure 17 shows three typical analog responses to charge injection for both a) a double sample and hold program and b) a quadruple sample and hold program. The points are measurements of V^{out} as a function of Q^{inj}. Note that here the SVXD chip inverts so that increasing collected charge results in a lower output level. The typical pedestal level is 2.5 V and the typical charge gain is 15 mV/fC. As can be seen from that figure, channel 219 is a good channel, with low leakage current: its response for a double or quadruple sample and hold mode is about the same, showing that the leakage current does not provide a significant amount of charge at the amplifier input. Channel 042 has a low pedestal in double sample and hold operation mode, due to a significant leakage current contribution; at high values of injected charge, the response even becomes nonlinear, indicating that the amplifier is starting to saturate. However, the leakage current contribution is reasonably taken out in the quadruple sample and hold mode, and channel 042 can be considered as a good channel when operated in this mode. Channel 197 has a very low gain both in double and quadruple sample and hold modes: it's a dead channel; the leakage current in this case is so big that it saturates the amplifier.

The measured gain spread within a ladder was typically ±5%. At this level the effect on clustering centroids is negligible.

10.2.2 Noise Measurement

The noise on the analog output of a given channel is defined as the standard deviation σ_v of the analog output voltage v for that channel:

$$\sigma_v^2 = \overline{v^2} - \overline{v}^2 \ . \tag{1}$$

Given the charge gain $G^{(Q)}$ of the amplifier this fluctuation can be expressed as a fluctuation of the input integrated charge,

$$\sigma_Q = \frac{\sigma_v}{G^{(Q)}} \tag{2}$$

which can be expressed in fC or in units of the electron charge.

The noise measurement is ideally a check of the electronic noise of the SVXD chip amplifiers. The expected value of this noise with a full 30 pF detector capacitance is shown in Figure 16 for quadruple and double sample and hold. These curves, determined under ideal conditions, with discrete capacitors, can be considered a performance standard. In a practical measurement with a real strip detector system this noise may be increased by a number of effects. These include coherent noise, or baseline shifts, interstrip capacitive coupling [34], and the effects of the finite risetime of the readout chip analog output. In a strip detector system these effects can be studied by varying readout timing and analyzing instantaneous correlations between separate or adjacent strips.

Coherent noise refers to a component which can be observed on many channels simultaneously. Because of the specific modes of operation of the SVXD chip, different sources of additional noise will appear in particular ways. The SVXD chip works by integrating charge in parallel on all inputs for a period of roughly 1 μs. Following this, each channel (or each latched channel) is then read out serially. Any one channel is typically driving the output bus for roughly 2–3 μs. The entire length of the readout scan depends upon the number of channels being read. For example, at full occupancy, a Layer 2 ladder would typically

require 1–1.5 ms. These two operating modes and time scales determine the susceptibility of the system to additional noise. High frequency noise which occurs during the parallel integration of charge will appear as a coherent shift on the analog output of all channels read out in a particular scan. A typical source of this noise would be fluctuations on the bias line of the silicon detector. The detector looks to the preamp as a capacitor in parallel with the input with a value of a few picofarads. Low frequency noise (such as 60 Hz line noise) which occurs during readout will also appear as a coherent shift on the analog output of all channels read out in a particular scan. Finally, noise with a frequency close to the readout clock but out of synchronization, will appear as incoherent noise on a sequence of read out channels. All these sources of additional noise can, to some extent, be limited by the testing setup, grounding, filtering, and power distribution systems.

Because of the potential susceptibility of the system to coherent noise, we defined also the "differential noise" of a given channel as $1/\sqrt{2}$ of the standard deviation of the difference between the analog output voltage v for that channel and the analog output voltage v' of a some other channel:

$$(\sigma_v^{diff})^2 = \frac{\overline{(v-v')^2} - \overline{v-v'}^2}{2} \tag{3}$$

The differential noise can also be expressed as a charge,

$$\sigma_Q^{diff} = \frac{\sigma_v^{diff}}{G(Q)} \tag{4}$$

and be measured for the two different modes of operation. Again, the differential noise measured with a quadruple sample and hold program is expected to be higher than the differential noise measured with a double sample and hold program by a factor $\sqrt{2}$. Assuming that $\sigma_v = \sigma_{v'}$, i.e., that the two channels have the same noise, we have

$$\begin{aligned}(\sigma_v^{diff})^2 &= \frac{\sigma_v^2 + \sigma_{v'}^2}{2} - \overline{vv'} + \overline{v}\,\overline{v'} \\ &= \frac{\sigma_v^2 + \sigma_{v'}^2}{2} - \rho\sigma_v\sigma_{v'} \\ &= \sigma_v^2(1-\rho)\end{aligned} \tag{5}$$

where ρ is the correlation between v and v'.

$$\sigma_Q^{diff} = \frac{\sigma_v\sqrt{1-\rho}}{G(Q)} \tag{6}$$

The differential noise is thus equal to the noise if there is no correlation between the analog output of the channels, and it is less(greater) than the noise if there is a positive(negative) correlation between the analog output of the channels. A positive correlation can be due to a common component of the noise induced by external pickup. A negative correlation can occur when the two channels are close due to the interstrip capacitive coupling. A simple model of this latter effect is shown in Figure 36 for the case of adjacent strips. With V_i equal to the instantaneous noise voltage at the *input* to channel i, σ_V the RMS of V_i (we assume to be independent of i), Q_i the instantaneous noise charge at the input to i, and σ_{Q_i} the RMS we have,

$$Q_i = C_s V_{i-1} - (2C_s + C_g + C_i + C_f)V_i + C_s V_{i+1} \tag{7}$$

$$\sigma_{Q_i} = \sigma_V\sqrt{2C_s^2 + (2C_s + C_g + C_a)^2} \tag{8}$$

with $C_a = C_i + C_f$ and

$$Q_i - Q_{i+1} = C_s V_{i-1} - (3C_s + C_g + C_a)V_i + (3C_s + C_g + C_a)V_{i+1} - C_s V_{i+2} \quad (9)$$

$$\sigma_{Q_i - Q_{i-1}} = \sigma_V \sqrt{2C_s^2 + 2(3C_s + C_g + C_a)^2} \quad (10)$$

The various capacitances are defined in the figure. For this case then the differential noise is

$$\sigma_Q^{diff} = \frac{\sigma_{Q_i - Q_{i-1}}}{\sqrt{2}} \quad (11)$$

and the correlation is,

$$\rho = 1 - (\frac{\sigma_Q^{diff}}{\sigma_Q})^2 \quad (12)$$

For two adjacent channels we called the differential noise *"D_{noise}"*. To completely isolate the effect of interstrip capacitance we called the differential noise calculated for a five strip separation the *"H_{noise}"*.

In Figure 37 we show calculated values of the *"D_{noise}"* versus interstrip capacitance based upon the model of Figure 36. In this calculation we set $C_g = 5$ pF and $C_a = 6$ pF. The effect of interstrip capacitance is second order and is only observable if the coherent contribution is well controlled. In the ladder testing process a coherent noise contribution was present and our measurement precision was limited by our readout electronics (8 bit ADC used with low gain). Typically the *"D_{noise}"* was 2400 electrons while the single channel noise was 2800 electrons. In the fully assembled detector, operating at the Fermilab Collider, the effects of capacitive coupling on the *"D_{noise}"* were observable. In that system we had good control of coherent noise and 12 bit ADC's. This will be discussed in Section 11.1 below.

A third effect which can play a role in noise analysis is due to the finite risetime of the analog output bus. In the case of the SVXD chip Rev. D we had $\tau = 800\ ns$. Because of this there will be a positive correlation between a channel and its preceeding neighbor in readout order (the *"readout effect"*),

$$v_{out}^i = v_{out}^{i-1 TRUE}\epsilon + v_{out}^{iTRUE}(1 - \epsilon) \quad (13)$$

where $\epsilon = e^{-t/\tau}$ and t is the length of the time the channel i is asserted on the analog output bus before digitization.

Again, in ladder testing this effect was not observable, but it was clearly seen during colliding beam operation of the full detector with minimal coherent noise and more precise electronics.

10.2.3 Sparsification Threshold Measurement

The sparse threshold measurement determines, for each channel, the mean value and the RMS of the amount of charge needed at the input of the front–end amplifier to set the latch. The results of this fundamental measurement allows us to decide which "operating threshold" voltage step V_{op}^{cal} should be sent on the calibration line when taking data with the SVX. The value of V_{op}^{cal} should be chosen to satisfy two requirements. The efficiency of sparse readout for the detection of particles crossing the silicon should be maximized. The number of noise hits (occupancy) read out should be minimized.

The RMS of the injected charge needed to latch a particular channel is a measure of the noise of that channel. This measurement does not use the analog information sent by the SVXD chip, and is an independent measurement of the noise of each channel, which, contrary to the noise measurement obtained from the analog data, will not be affected by any eventual contribution of the testing setup (port card, cables, receiver and ADC).

The sparsification threshold measurement consists of measuring a finite number of points on the "efficiency curve" (Figure 38) of each channel (which is effectively the integral of the pedestal distribution, assumed here to be a gaussian distribution). The probability to latch is measured for various values of the injected charge. To perform these measurements, the calibration voltage pulse is stepped through N different values, equally spaced between a value V_{low}^{cal}, where (almost) all the channels don't latch, and a value V_{high}^{cal}, where (almost) all the channels do latch. At each step i, the calibration voltage pulse is set to

$$V_i^{cal} = V_{low}^{cal} + (i - \frac{1}{2})\Delta V^{cal} \qquad i = 1, \ldots, N \tag{14}$$

where

$$\Delta V^{cal} = \frac{V_{high}^{cal} - V_{low}^{cal}}{N} \; . \tag{15}$$

Typically, ΔV^{cal} is taken sufficiently small to measure a few points on the curve and is in the range 5–10 mV. A data acquisition program performing a quadruple sample and hold and enabling the "positive sparse" logic is run in the SRS, and a number N_{evts} of events are read out during a given step i; for each channel, the probability to latch, ε_i, is estimated as

$$\varepsilon_i = \frac{N_{latch}}{N_{evts}} \tag{16}$$

where N_{latch} is the number of times the address of that channel is present in the data collected on the digital lines during the current step (note that the analog data is not used).

At the end, the sparsification threshold, V_{thresh}^{cal}, and its RMS value, σ_{thresh}, are estimated using the following formulae:

$$V_{thresh}^{cal} = V_{low}^{cal} + \Delta V^{cal} \sum_{i=1}^{N} (1 - \varepsilon_i) \tag{17}$$

$$\sigma_{thresh} = \Delta V^{cal} \sqrt{\sum_{i=1}^{N} (2i - 1)(1 - \varepsilon_i) - \left(\sum_{i=1}^{N} (1 - \varepsilon_i) \right)^2} \tag{18}$$

Figure 39 and Figure 40 show the percentage of dead and noisy channels as function of the ladder number. Here noisy is defined rather liberally as having more than a 20% probability to latch during sparse readout. Most of the ladders have less than 2% dead channels and less than 5% noisy channels.

During operation of the SVX detector with colliding beams, the sparse threshold measurement was part of a standard set of calibrations. This process and the long term behavior of the sparse thresholds is discussed in Section 11.1 below.

10.2.4 Recovery of Damaged Strips

In the course of prototyping and constructing ladder modules for the SVX we observed that strips with a sufficiently large leakage current would share that current with neighboring

strips in proportion to the distance between them. Because of the characteristic pattern of this sharing we called these areas "black holes".

A working hypothesis is that the black holes are caused by the phenomenon of punch-through in a p^+np^+ structure [35] but only occur here because of the way the SVXD chip behaves when it becomes saturated.

For an integrated charge of about 60 fC the SVX integrator will saturate. The normal reset point of the integrator is 1.1 V. Once it saturates, the input can charge up to 6 V plus a diode drop. At that point protection diodes, which connect the inputs to the AP=6 V line, will turn on and the input will be fixed at that level. Under this condition, in the vicinity of a damaged or high leakage strip, with the neighbors all at 1.1 V, sizable interstrip current can apparently flow. Depending upon the magnitude of the current injected, the neighbors may even saturate as well. This will create a cascade like effect which may affect finally a large number of strips. An example of this is shown in Figure 41a, a double sample analog output offset plot which is directly proportional to the strip leakage current.

We found that the black hole effect required a strip leakage in excess of a few hundred nA for our typical integration times. We also observed that leaving a known leaky strip unbonded prevented in most cases the black hole from appearing at that location. Since the integrator saturated anyway at about 60 fC we chose to leave all strips with current in excess of 70 nA unbonded. Occasionally, in the case of a very leaky strip, a black hole was observed centered on that strip, although it was skipped during wirebonding. This kind of black hole could be fixed by connecting the bad strip to ground.

During the wirebonding process another class of high leakage strips appeared. These were due to damage to the detector in the bonding process. In particular, when the bonding tool hit the silicon dioxide the effect was particularly pronounced. Subsequent removal of the bond wire at that strip generally did not remove the black hole. Instead the seed strip just moved to the next bonded strip.

To understand these patterns we consider the various sources of excess leakage current. Those strips which were delivered with high leakage probably contained a defect induced during ion implantation of the p^+ regions. This defect is perhaps a micron below the surface. Consequently, if the strip is unbonded the defect may remain in a relatively low field region and not contribute carriers to the neighbors. Those strips which have instead surface damage due to bonding may contribute a large surface current which persists even if the nearest strip is floating, as long as the surface is depleted. That current will just sink to the nearest bonded strip.

In the case of the persistent black holes we found that the current could be satisfactorily drained if the strip was connected, via a low impedance, to voltage level near the nominal 1.1 V reset point of the integrator. Connecting it to ground would not do as the black hole then just inverted and became a peak. This worked as long as the impedance was smaller than the apparent impedance into the saturated preamplifier. The same apparent draining effect came about if the offending strip was instead grounded through a capacitor of value in excess of 0.1 μF. Apparently at the frequency of preamplifier resets the capacitor both maintained the right potential at the strip and also drained the current sufficiently. This was the final procedure used in production for these strips. The effect of this bonding can be seen by comparing Figure 41b (after 2 black hole bonds) with Figure 41a (before black hole fixing). Generally, the two neighboring strips around a black hole would show increased noise after black hole fixing using this procedure but were still active.

10.3 Mechanical Assembly of Barrels and Optical Alignment

The final assembly of ladders into the bulkheads is done on a rotating shaft assembly using a CMM. This assembly was called the *"Barrel Fixture"*. The barrel fixture was constructed on the granite measuring table of the CMM. During construction it was surveyed and aligned using the CMM. This fixture consisted of four upright beams and two cross beams which supported a rotating steel shaft. The SVX bulkheads were attached to steel wheels *"wagon wheels"* which were then rigidly connected to the rotating shaft. This is illustrated in Figure 42. Figure 43 is a photograph of a partially assembled barrel on the assembly.

When the SVX is installed in CDF it rests on supports within the VTX through a classic three point kinematic mount. Before attaching the bulkheads to the wagon wheels they were individually surveyed on the CMM and then the SVX side of the kinematic supports were epoxied to the bulkheads. The bulkheads were then mounted and aligned on the wagon wheels and locked into place with small dabs of structural epoxy.

The bulkhead–wagon wheel composites were mounted and aligned on the rotating shaft of the barrel fixture using the CMM. Measurements were made as the wheels were rotated in order to calibrate a shaft encoder system on the fixture.

Ladders were mounted on the barrel starting with the innermost layer. The strips of the silicon detectors were measured directly with a TV camera on the CMM to an accuracy of 2.5 μm. The layer of ladders nearest and farthest from the beamline are oriented so that the detector strips face the beamline and thus measurements can be made only of the back edges and corners of the detectors after assembly into the barrel. For these two layers, the edges and corners have been referenced to the detector strip locations from measurements done prior to installation.

As the barrel rotated on its construction fixture in going from wedge–to–wedge during the optical survey, there was observed a small wobble in the shaft which affected the measurement of the absolute position of the ladders. This was an effect introduced by the fixturing and needed to be removed to give the actual location of the ladders in the barrel. The effect of this wobble was different at the readout and dummy bulkhead positions and changed with the orientation of the barrel. This runout was measured by recording the position of bulkhead rims relative to a fixed point in space, as the bulkhead was rotated. The effect of the runout was removed relative to a default orientation of the barrel. The runout corrections are non–negligible, with the largest correction being 60 μm. The runout was measured several times and an average value was taken. All of the optical constant values have been corrected for runout.

Figure 44 shows the repeatability in the measurement of the position of the silicon detector strips for all ladders installed in the SVX detector. This distribution was determined by taking the difference of two measurements of the detector strip positions during the barrel construction and has an RMS of 4.2 μm, which is consistent with the repeatability of the measuring device. In addition to the strip measurements, the bow or radius of each ladder is measured along its length using the CMM. Figure 45 shows the maximum bow or sagitta of all ladders in the SVX detector. The average value is 23 μm and will have a negligible contribution to the SVX detector position resolution.

After the ladders were installed between the bulkheads, port cards were mounted at the outermost radius. Bus cables were installed between the ladders in a wedge and full electrical tests were performed. A view of the detector at this stage is shown in Figure 19. Following this a lightweight composite cylinder, consisting of 1 mm of Rohacell wrapped in 75 μm of aluminum foil, was slid over the barrel and was glued to both bulkheads. This cylinder

and its connection to the bulkheads serves to maintain the internal mechanical alignment of the ladders after the barrel is removed from the wagon wheels and also provides shielding to and from stray RF fields. In addition, it isolates the SVX detector both thermally and electrically (DC) from the surrounding tracking chambers.

After release from the wagon wheels a thin (75 μm) inner foil screen was inserted through the center bore. This serves to protect the SVX from electrical pickup off the beampipe and against mechanical damage during insertion into the CDF tracking volume.

The SVX was suspended inside the VTX by a fixed, three–point, kinematic mounting system. Such a system avoids introducing stress on the SVX barrel that might induce unwanted distortions, while rigidly constraining the detector. All SVX cables were dressed and taken out through a split between the two VTX modules at z=0 (see Figure 46). We chose to take the cable out this way to minimize material a small radius and at small angles with respect to the beam direction. The entire SVX/VTX assembly was then inserted into the CTC on a pair of carbon fiber rails on the VTX that engaged a set of precision linear bearings located on the CTC tube. Dowel pins fixed the final position of the assembly along the z–axis. Demanding tight tolerances in the rails and bearings slightly over–constrained the VTX, resulting in a rigid mount. The assembly was installed by sliding it over a pre–positioned stationary beampipe. The inner layer of silicon is at a radius of 1.177 in. from the beam and is thus $<$ 0.5 in. from the surface of the 1.5 in. outside diameter, 0.020 in. wall thickness beampipe.

10.4 Installation Survey

The process of installing the SVX first into the VTX, then into the CTC was monitored by a series of optical surveys. The purpose of these surveys was twofold: first, to verify that the mounting system met design goals of placement accuracy and reproducibility, and second to establish the actual mount position of the detector with sufficient precision to serve as a starting point for further analyses using tracking data. In addition, since the sensitivity the track–based analyses to the detector z position is low, the optical surveys provide essentially the only measurement of the z position.

The mechanics of installing the detectors precluded direct position measurements after final installation. For this reason, an important design objective of the mount system was to achieve a high degree of reproducibility in the final detector position through repeated insertion/extraction procedures. Surveys conducted after two such cycles found no evidence for position shifts transverse to the barrel axis down to the level of 75 μm, the precision of the measurements. Shifts along the barrel axis were on the order of 250 μm, again at the level of measurement precision and well within design tolerances.

An incidental shutdown during data–taking afforded an independent check of the detector mount reproducibility. During this two–week period, the SVX–VTX assembly was extracted and re–inserted. Track–based analyses of data taken before and after the shutdown confirmed the optical survey findings.

Results from the final detector surveys are parameterized as displacements from the nominal position and orientation of the barrels. The angles α, β and γ represent rotations around the y, x and z axes, respectively. To obtain these alignment parameters, we first measured fiducials located directly on the bulkheads using the high precision CMM discussed earlier. These measurements provided a precise reference between the fiducial points and the internal coordinate system of the detector. Once the detector was fully mounted and inserted, the fiducials were again surveyed. Measurements from this survey were fit to the

precise results from the CMM to obtain the alignment parameters. Results from the final detector surveys were consistent with those from all earlier measurements, except for an internal inconsistency of about 1 mm in the z position of the east barrel. The measurement resolution of the detector is not sensitive to z translations of this magnitude.

11 Online Performance and Calibration

11.1 Performance Monitoring

First level monitoring of the SVX used an online event display which sampled data written to tape. This display ran whenever data taking was in progress. An example of an event is shown in Figure 47. Early problems could often be caught at that level and diagnosed. Routine monitoring of the SVX include the following calibration procedures: pedestals, noise, and D_{noise}, gains, thresholds, and leakage currents. These quantities and the algorithms used to calculate them are described in detail in Section 10.2. Typical calibration results are shown in Figure 48 through Figure 51.

As discussed in Section 10.2, it is possible to separate the effects of coherent noise, interstrip capacitive coupling, and the finite risetime of the analog output (*"readout effect"*) by varying timing and studying instantaneous noise correlations between channels. During operation of the SVX with colliding beams we limited the readout clock period to 2400 ns per channel for the analog readout. Consequently ϵ of Equation 13 was 0.05. This led to a measurable readout effect which in principle will bias cluster positions for tracking. In practice the shifts are small and are taken out automatically as an apparent misalignment layer to layer. To isolate the remaining effects due to coherent noise and interstrip coupling we increased the readout period to 10000 ns for the purpose of a study. The result of this study is shown in Figure 52. For the full detector in operation the coherent noise is less than 600 electrons. The measured correlation coefficient after removal of the coherent contribution is about –0.3. Referring to Figure 37 we see the expected value for a reasonable estimate of our interstrip capacitance (10–13 pF) is considerably different. This may be due to additional frequency dependent effects not included in the model of Figure 36.

The procedure for determining sparse readout thresholds was discussed in Section 10.2.3. In practice this measurement is performed on–line as a standard calibration of the detector. From this we determined 48 values of V_{op}^{cal} to use during data taking. Reliable operation of sparse readout required short term stability of these operating points, only small variations of V_{thresh}^{cal} within the segmentation set by the fixed number of threshold inputs, and no significant coherent noise in the system. As discussed above, the coherent contribution was small. In Figure 53 we show a scatter plot of the thresholds (50% efficiency points) and RMS (σ_{thresh}) for all channels in a wedge. The units are arbitrary but the scale is set by the RMS. All threshold variations should be of that order. Finally in Figure 54 we show the variation in the threshold and σ_{thresh} over the full course of the collider run. The thresholds were remarkably stable.

The threshold uniformity and the segmentation of the threshold loading inputs determines what occupancy can be established for a given hit efficiency. For SVX, chip to chip variations due to parasitic charge injection was a limiting factor in minimizing the occupancy. While we operated within the CDF specified event size and readout time, it is worthy to note here this effect. Before incurring radiation damage, we operated with typically 5–6% occupancy mostly due to the threshold variation along the wedge. After radiation damage, we purposely lowered the operating points to increase our efficiency. By the end of the run

we had 15–20% occupancy, which was dominated by the inner most layer. In Figure 55 we show a plot of occupancy on an inner layer (beam off) versus V_{op}^{cal} (plotted here in electrons) before and after radiation. Also shown is simultaneously a measure of the latching inefficiency. This quantity is defined somewhat arbitrarily. Here it is the probability for a signal of half an average MIP to latch. The true inefficiency is given by this convoluted with the pulse height distribution for all tracks and is therefore much smaller. Our operating points before irradiation were determined by minimizing the sum of the two low dose curves shown in the plot. In fact, most of the occupancy in the detector was due to fixed variations in the sparse thresholds within a wedge. In Figure 56 we show a (pre–irradiation) distribution of event occupancy for a typical wedge both for beam on and off conditions.

The occupancy is also affected by how well leakage current variations from strip to strip are removed by the quadruple sample and hold. Referring to the ΔT effect discussed in Section 5.1, we show in Figure 57 the occupancy for a wedge versus the time difference between first and second integration. This occupancy was measured early in the run for beam off conditions. The clear minimum occurs close to the expected value.

The most occupied SVX wedge determines the total scan time required to readout the detector. Even at the end of the run, with occupancies on certain wedges approaching 20%, we remained below the CDF required readout time of 2.2 ms. The effect of occupancy on readout time is discussed in more detail in Section 7.5 and indicated in Figure 32.

11.2 Calibration Procedures

There are two modes of calibration used in CDF, D–mode and X–mode. D–mode is identical to the normal data–taking mode in CDF, where events are taken one by one, with each event generating an individual output data bank. For SVX calibrations, this means that each event generates a bank containing data for all 46080 channels. This is both time–consuming and computer intensive. X–mode is used for most SVX calibrations. In X–mode, intermediate sums of the relevant calibration quantities are made in the SSP's. Only these sums are output, saving both time and offline computer resources.

For instance, a typical D–mode gain run has 10 steps in VCAL, with 50 events taken per step. This gives a total of 500 events, each with an output bank containing 46080 channels. When analyzing the data, the offline computer must read and process all 500 events. In X–mode gain, the SSP's sum the ADC counts and square of the ADC counts for all 50 events in a given step. For each step, one set of output banks is made. containing a total of 46080 channels. When analyzing the data, only 10 sets of banks have to be read in, where all sums have already been computed. This results in a factor of ten reduction in data size, and saves a factor of two in offline elapsed time.

In normal operations, pedestals are taken in D–mode. This is because D_{noise} cannot be calculated from the X–mode output. In addition, D–mode allows for checks for dead channels in the SVX. This is done as part of every pedestal run. X–mode is used for all other SVX calibrations.

Nominally, SVX calibrations are performed according to the following schedule: pedestals are taken at least once every two days, gains and thresholds at least once a week, and leakage currents every few days. Towards the end of the run these frequencies increased. These calibrations are an important monitor of the SVX performance at any given time. They provide a history of the radiation damage to the device and changes due to environmental conditions.

Since the SVX is rather stable, it is not necessary to update the calibration constants

frequently. The pedestals are typically updated in the CDF database only every week. While there are long term shifts (due to radiation), on the one week time scale there are not serious shifts. This stability means an extremely large calibration history database is not required for the 46080 channels of the SVX.

12 Radiation Damage and Monitoring

12.1 Expectated Dose

The performance of the SVX detector could be compromised by beam related radiation damage to the readout chip and silicon detectors. The expected effect of radiation on the SVXD readout chip is described in Section 12.2 below. Based upon these effects we adopted an upper limit of 15 KRad as the tolerable integral dose for the SVX running period. Measurements of beam related backgrounds were made during the 1988–89 CDF data run. Thermo–luminescent dosimeters (TLD's) were mounted close to the beam pipe within the central CDF detector, about 2 m from the interaction point, and extracted at approximately monthly intervals. We normalized the reconstructed dose to delivered luminosity, although it is clear that we may be averaging over burst like doses from accelerator accidents. The TLD record shows an an average exposure of about 900 rads per pb^{-1} at startup, declining to 300 rads per pb^{-1} by run end, suggesting the presence of both "commissioning" and "steady" components in the dose. Extrapolating to the expected of exposure of 25 pb^{-1} for the SVX data run, the integral expected dose is approximately 12 kRad, which has very little margin with respect to our upper limit. In addition, the high doses recorded during Tevatron commissioning raise a spectre of uncertainty regarding the possibility of single fatal accidents.

In order to protect the detector from single accidents and also to aid the accelerator operators in tuning the Tevatron we developed and installed a real time radiation monitoring and abort system for CDF. This system is described in Section 12.3 below.

12.2 Anticipated Radiation Effects

Radiation damage to silicon detectors has been discussed in the literature [36]. Measurements have been made with a wide range of particles and spectra. Charged hadron damage constants for leakage current increase lie in the range $1.3 - 9 \times 10^{-8}$ nA/cm. Damage constants for low energy neutrons are higher. It is difficult to directly apply any numbers to a particular accelerator environment since the energy spectrum and particle mix are poorly known there. Our expectations for damage to the silicon detectors are based upon the range of damage constants reported. From these data and our TLD estimate of 300 Rad/pb^{-1} we expect an increase in detector leakage in the range 30–100 nA/strip for the 25 pb^{-1} exposure.

The DC coupled SVXD readout chip preamp will saturate for currents in excess of 80 nA unless counter measures are taken. For example, a reverse charge injection can be applied during data taking to cancel the integrated current. Increased leakage will also add a shot noise contribution to the preamp output. At 80 nA this will be approximately 850 electrons.

Radiation damage to CMOS readout electronics is primarily due to the creation of electron–hole pairs in the transistor gate oxide and subsequent trapping of charges and to the creation of interface states. By varying the processing technology it is possible to make

CMOS more or less susceptible to these effects. In the case of the SVXD readout chip the technology was entirely radiation soft.

To understand what the actual damage would be, a set of irradiations were performed on test chips before the run. The irradiations were done using a ^{60}Co source at Lawrence Berkeley Laboratory. This source delivered about 3,000 Rad per hour at 1 m (the measuring position), and the samples were irradiated with a dose rate which never exceeded 10 KRad per hour.

During irradiation, the samples were mounted perpendicularly to the source with a screen of aluminium and lead (1.5 mm and 0.5 mm thick respectively) in front of the chips in order to reach the "charged particle equilibrium" [5]. The chips were exposed both with the power on and the power off. This was done to determine whether the radiation damage to the CMOS was worse under power and to justify a proposed power down procedure during lossy operations of the accelerator. In order to simulate the presence of the silicon strips three preamplifier inputs per chip were connected to capacitors of 10, 20, and 30 pF respectively. Measurements were performed on four devices while a fifth was held unexposed as a control. In addition to the irradiated chips, a set of test transistors included in the SVX die were studied in order to correlate observations with fundamental transistor parameters.

In Figure 58 the change in the overall gain of the chip as a function of the radiation is shown. To understand the gain changes, we refer to the circuit diagram of Figure 14. The integrator gain is set by a passive device while the subsequent voltage gain stages are operated open loop. The observed loss of gain with dose is due to a decrease in transconductance for transistors in the voltage gain stages. It is also higher for the power on than for the power off measurements. The observed fall is about 30% after 30 Krad. This is also consistent with the decrease of the transconductance measured on the single transistors.

Using a probe station we measured the gain of the different stages before and after irradiation and found that the gain losses are distributed among the open loop stages and do not affect the gain of the charge sensitive preamplifier as expected.

The output noise spectrum of a CMOS amplifier is dominated at low frequencies by the $1/f$ noise and by the white noise at higher frequencies. Both these components are affected by radiation due to trapped interface states in the input transistor.

In our measurements, shown in Figure 59, the noise level referred to the input of the integrator is increasing with the dose with no significant difference between power on and power off measurements. The increase is such that the noise doubles after 30 KRad on the 30 pF input channels. The result indicates some saturation at higher doses.

Based upon these expectations for increase in leakage and noise we set 15 KRad as an upper limit on *"acceptable"* dose during the commissioning period and data taking run.

12.3 Monitoring and Abort System

Radiation backgrounds are monitored with two systems of detectors placed about 2 m from the interaction region in both the upstream and downstream proton directions. At each station, the instantaneous minimum ionizing particle rates are measured by a set of 3 silicon PIN diodes arranged symmetrically around the beam pipe, and ionizing dose levels are measured with two Tevatron Beam Loss Monitors (BLMs)[37] placed on the inside and outside of the beampipe in the plane of the accelerator. The BLM is a sealed glass ion chamber with very low leakage currents which is read out by a logarithmic integrating amplifier with a time constant of 100 ms. The system has good linearity and a calibrated response over the full interesting range of 0.1 to 100 Rads/sec. The final component in each

monitor station is a thin G10 disk which carries an array of thermo–luminescent dosimeters (TLDs) which can be extracted at quasi–monthly intervals for cross calibration.

Rate and dose information from the monitors are processed with a CAMAC based system developed in conjunction with the FNAL Accelerator Controls Division. Rate information is processed via 3 digital ratemeters with integration on 5 KHz, 500 Hz, and 5 Hz scales, synchronous with the Tevatron beam clock. Ionizing dose information is sampled at 5 KHz and compared to programmable alarm and abort thresholds. The rate and dose information is loaded into circular buffers of 2K samples which can function as high resolution snapshots around beamloss events of interest. In addition, the dose buffer is read into a companion processor which integrates the total exposure. Sampled information is also directly readable at slower speeds for archive to history files. The system is embedded in the Tevatron control structure, and interfaced to the Tevatron abort loop.

Figure 60 shows an example of this system during a Tevatron abort. The abort is brought on because of large losses into the SVX monitors. In Figure 60 part A, the curve labeled "Quad Current" monitors the current in a final focus quadrupole. In this instance, the current was being adjusted to study the accelerator β function and it passed into a region of unstable beam. The beam current, labeled "Intensity" in part B, drops to zero because of an SVX initiated abort. The total dose recorded by the BLMs, show in Figure 60 part C, is approximately 30 rads. This particular accident was one of the largest seen during the Tevatron operation. The time structure of the dose in the 400 ms before the beam was aborted was saved in the circular buffers and is displayed in Figure 60 part D.

Figure 60 part D also demonstrates that good protection at the Tevatron does not require extremely fast decisions. In fact, we discovered that a certain integration was necessary in order to eliminate needless aborts on fast but low dose transients, such as those that occur during bunch injection. The 5 KHz ratemeter system, intended for protection against hypothetical "fast" accidents, was eventually removed from the abort loop.

Figure 61 shows the currents and loss monitors over the course of normal Tevatron colliding beam cycle. The three plots in this figure show the current in a final focus quadrupole, the instantaneous luminosity, and the integral dose to the BLMs. We show an hour of the cycle, covering the beam injection, acceleration to 900 GeV, the "low beta squeeze", and the stable beam time. The beam injection and acceleration occur during the first 10 minutes displayed, giving very little integrated dose. The *lowbetasqueeze*, which occurs between 15 and 20 minutes into the cycle, is the point at which the losses were the highest. The total dose was minimized by performing this operation as fast as possible. Once the beams were focused, they were brought into collision and losses were stabilized (the time period 20 to 25 minutes into the cycle). Note that the loss rate went down significantly during this time period while the luminosity reached its maximum value. The final 35 minutes displayed show the steady dose rate associated with the particle flux from the beam collisions.

12.4 Dose Measurements

The radial dependence of the integral dose at the monitor stations is reconstructed from the TLD record, and found to behave approximately as $r^{-1.5}$. The TLDs are used to calibrate the BLMs, which then provide a complete time history of the radiation dose. The measured radial dependence has been used to extrapolate to the radius of the first SVX layer (L0 at 2.99 cm), but the monitoring station is actually 2 m downstream from the SVX. The doses measured here are higher than at the SVX position. The correct relationship between these two locations is not known. We choose to use the noise degradation of the SVXD

chips as a final normalization to get the estimated ionizing dose at the SVX position. The observed values imply the dose at the monitoring station is 3 times higher than at the SVX. The time history, in Figure 62, shows some steep ascents during the initial stages of Tevatron commissioning, and then a steady climb related to the reliable delivery of luminosity. When the dose is plotted against constant intervals of delivered luminosity, as in Figure 63, we see that more than one third of the total dose to the SVX occurs in the first tenth of integrated luminosity, followed by a break to a linear regime where the dose of approximately 300 rads per pb^{-1} is in agreement with the measurement from the 1988–1989 run. The operational experience here is that the accelerator startup was plagued by high losses and SVX aborts until the Tevatron was tuned to operate with low losses near CDF. We emphasize that the total dose is quite small compared to what one might have expected at a hadron collider. In an operational context, the use of this monitoring system created a new channel of communication between the experimenters and the accelerator operations group. This collaboration worked well and, as a result, dose to the SVX was minimized. Indeed the accelerator was tuned to achieve relatively "lossless commissioning", and ultimately, very clean running.

12.5 Radiation Effects on the SVX Detector

Clean running and low losses at injection not withstanding, beam–beam collisions at CDF are the source of an irreducible radiation dose to the SVX. The effects of this dose on the detectors and readout chips became clearly visible once high luminosity running began. As discussed in Section 12.2 above, radiation damage should cause detector leakage currents to increase, front end readout electronics noise to increase, and gain to decrease. Quantitative expectations are based upon measurements which are typically done with other sources of radiation and over shorter time scales. Since doses at CDF are integrated rather slowly, annealling effects may be important as well. Below we discuss first the basic observed changes to the detector performance. Following we describe higher level effects on the offline reconstruction of data from the SVX in the presence of radiation damage.

12.5.1 Hardware

For simplicity we focus on one particular wedge which was relatively free of any other problems which might obscure radiation effects. In Figure 64 we plot the leakage current averaged over each layer versus integrated luminosity. The flattening out and slight decrease seen at an integrated luminosity of 13 pb^{-1} occurred during a 10 day shutdown of the accelerator and may perhaps be interpreted as self annealing of the damage. In Figure 65 we plot the front end chip charge gain, averaged over each layer, versus integrated luminosity. The small dip seen is due to a change in algorithm and should not be interpreted as a real effect. In Figure 66 we plot the front end noise, corrected by the measured gain, averaged over each layer versus integrated luminosity. The expected qualitative trends are apparent. Of particular note is the noise increase of 50% on the innermost layer. In Figure 67 we plot an inferred dose based upon the observed changes in gain and noise versus luminosity. This inferred dose uses the data discussed in Section 12.2 as a *"calibration"* so the noise data does not contain any new information. The gain variation is inconsistent with the noise variation. In the case of leakage current it is difficult to compare with damage to the readout chip since bulk silicon and CMOS are sensitive to different radiation components and spectra. Given this caveat, we plot, in Figure 68, the observed leakage current increase

versus the dose derived from the noise increase.

12.5.2 Offline Data

We studied the effect of radiation damage on tracking performance by increasing the strip noise in a Monte Carlo simulation. The amount of additional noise in each layer followed a radial dependence determined from TLD measurements.

As expected, the track quality decreased as simulated dose increased. The fraction of reconstructed tracks with 4 associated SVX hits decreased as more noise was added since the clusters formed on the inner–most layer were of poorer quality or were not reconstructed as clusters at all. The fraction of "junk" tracks, those with unlikely hit patterns and large track chi–squared, increased with more noise. The application of a stringent track quality requirement recovers the nominal impact parameter resolution but at the expense of efficiency. The net efficiency loss to maintain constant resolution on passing tracks is shown as a function of the noise increase in Figure 69.

Modifications to charge clustering thresholds were found to be ineffective in addressing the problem. While tighter clustering requirements did reduce the number of junk tracks, it also decreased the number of good tracks. Conversely, lowering the cluster thresholds did not recover good tracks lost due to radiation damage, but did allow more junk tracks to be constructed. This issues are discussed further in Section 14.

13 Operating Experience

13.1 Detector System Interference

As discussed in Section 3.1, the SVX detector was mounted inside both the Vertex Time Projection Chamber, VTX, and the CTC. The timing signals which controlled the sample and hold operation in the SVXD chip had to arrive just prior to beam crossing time. After the SVX was installed pickup was observed on the sense wires of both the VTX and the innermost CTC wire layers. This pickup was clearly correlated with switch transitions in the SVX timing signals. The picked up signal, when probed at the output of the wire chamber preamplifiers, was a damped oscillation which decayed to 10% of its maximum in roughly 300 ns. The oscillation frequency was a property of the wire chamber preamplifiers. This pickup, and its effect on the other tracking systems, was reduced to an acceptable level by a number of measures. The SVX cables passed over the outer surface of the VTX in close proximity to unshielded lines which supplied bias voltage to the chamber. The SVX cables were wrapped in aluminized kapton shields which were grounded at one end. By adding additional ground strap between the shields and local preamp signal ground for the VTX, a significant improvement was made. In the case of the CTC pickup, grounding improvements were made for that system's readout electronics which eliminated pickup from the SVX. Finally, the SVX clock, which preceeded beam crossing, was moved 300 ns earlier to be further out of the sensitive drift time period of the tracking chambers.

After the noise reduction due to the grounding of shields on the VTX, it was observed that the pickup was also reduced when the SVX port cards and front end chips were powered down. Furthermore, the residual pickup was observed to occur primarily in those regions of the VTX closest to the SVX barrels. Note that the SVX cables run along the entire length of the VTX ($\approx$ 140 cm/module) while the barrels themselves only occupy the central 26 cm/module. These two facts suggest that the remaining source of pickup are the

SVX electronics rather than the cables. For example, use of fiber optic data transmission techniques would not necessarily improve things in this case. Better would be the use of differential drivers and receivers with smaller signal transitions or more extensive shielding around the SVX barrels.

13.2 Failure Modes

In a complex system like the SVX some level of failure is inevitable. An attempt was made in the design and construction of the device to insulate the system from certain failure modes. For example the wedge based readout configuration was chosen in part so that if a cable or port card failed at most 4.5 % of the SVX acceptance would be lost. In fact the failures which did occur were much less significant than that. For the sake of future applications of this technology we will list them here.

All signals came into the SVX port card on differential pairs. On one port card one side of a pair apparently opened. This pair supplied a DC calibration voltage to the charge injection circuit for the innermost layer of that wedge. The circuit still functioned but the calibration voltages were doubled in compensation. No increase in noise was seen in spite of the single ended operation.

One SVXD chip on Layer 1 of a wedge failed to give analog data. Apparently one of the connections to a sample and hold switch was lost. Fortunately it continued to function as a member of the control and readout daisy chain so that all the other chips in the wedge were not effected.

One SVXD chip on Layer 1 of a wedge could not be put into Latch All mode. This complicated pedestal measurement but a method around that was developed so there was no real problem in the end.

One SVXD chip on Layer 1 of a wedge functioned properly for analog readout but gave incorrect channel address and chip ID readback. There was a particular pattern to these digital errors and for the most part the addresses could be recovered offline.

A number of chips gave occasional illegal chip ID readbacks. Most of these could be recovered offline.

The apparent concentration of chip hardware problems on Layer 1 is not understood as a systematic effect since the problems are all different.

Occasionally, large pedestal shifts were seen in small regions of the detector but they were generally short lived. These could be due to the external DAQ system as well.

13.3 Leakage Currents

In late October 1992 (4 months into the run), certain ladders in the SVX began to experience sharp increases in leakage current. The increase was large enough to bring the preamps close to their saturation point, thus decreasing the effective gain. These drops in gain resulted in isolated low–efficiency regions in the detector. The redundancy provided by four tracking layers enabled the SVX to continue operation despite these problems. However, the currents were increasing, and continuing to operate with these high leakage ladders was questionable.

The cause of the change in leakage current is not understood. It is believed to be due to surface effects on the silicon wafers. In general, the affected ladders were those which had particular moisture sensitivity during construction (see Section 10.2). In Figure 70 we show an example of this effect. One hypothesis is beam related particles ionize the argon–ethane gas surrounding the SVX. Charge then collects on the surface of the detectors, producing

high leakage currents. The increase in leakage current is correlated with beam activity in the Tevatron. Leakage currents seem to increase most during Tevatron beam squeeze, when the particle loss is high. Without beam, the currents tend to decrease. The rate of decrease is greater when the silicon is left at full bias voltage, possibly because the surface charge is then being dissipated. In Figure 71 we show the total current on a ladder over many days of time. The correlation with beam and improvement with time is apparent.

Up to November 1992, the silicon bias voltages were ramped down to 4 V when not taking data. This was done to minimize the chance of tripping the bias supplies during Tevatron studies, beam injection, and tuning. In mid–November 1992, this procedure was modified to help control the currents on the high leakage ladders. The high leakage ladders were thereafter kept at full bias at all times.

The increase in leakage currents may also be due to the gas volume surrounding the SVX. The SVX sits inside the argon–ethane gas volume of the CDF Vertex Detector (VTX). Because of this direct coupling between detectors, major changes to the gas system, such as surrounding the SVX with a dry nitrogen atmosphere, could not be made. Instead, minor modifications to the VTX+SVX gas system were attempted. The argon–ethane supply to the VTX+SVX was isolated from the CDF main supply, in case there were some contaminants in the main supply to which the SVX is particularly sensitive. To remove possible isolated pockets of stagnant gas around the SVX, the argon–ethane flow directly onto the SVX was varied. None of these modifications had a clear effect on the high leakage current ladders.

During a one week shutdown of the Tevatron in January 1993, the VTX+SVX system was switched to dry nitrogen. The belief was this change in gas, coupled with the fact that the SVX would be at full bias with no beam, would help lower the currents on the high leakage ladders during the shutdown. Instead, the change in the high leakage ladders was minimal compared to just before the access. In fact, when the VTX+SVX system was switched back to argon–ethane in preparation for the return of Tevatron beam, the high leakage ladders showed a much greater rate of improvement. It is not clear why this would be the case. The VTX+SVX system thereafter used the CDF main argon–ethane supply.

Certain ladders continue to show higher than average leakage currents, but not enough to seriously affect the performance of the SVX. By keeping the affected ladders at full bias all of the time, the problem has been kept under control.

14 Offline Performance

SVX reconstruction code must perform a two step process to go from the raw charge levels from the data acquisition system to the objects (tracks) used for physics analyses. The first step is the conversion of the charge levels on individual strips to clusters, where we take into account the calibration pedestal and noise values for each channel. In the second step, these clusters are linked to segments found in external tracking chambers to form the final tracks.

14.1 Raw Data Reduction

The conversion from charge levels on individual strips to clusters begins with an offline pedestal subtraction. We do a strip by strip pedestal subtraction, rather than an average pedestal subtraction, to account for any variation between strips. This choice requires having the full 46080 channel pedestals available.

Pedestals were regularly measured as part of a standard calibration procedure as described in Section 11.2. These pedestals were read in latch–all mode (Dpeds). Systematic studies indicated that these pedestals differ from the actual pedestals which exist for sparse data (Physpeds). Sparse data pedestals can be determined by calculating the pulse height distributions of neighbors strips of noise hits from colliding beam data. There is a small bias in this sample since noise anti–correlates between adjacent strips. Sparse pedestals and Dpeds were found to differ initially by about 2000 equivalent input electrons (or 1 noise σ). This shift grew considerably with radiation damage to the inner layer in particular. By the end of the run these pedestals differed by about 10000 electrons on the innermost layer. At that point, use of Dpeds had a serious effect on hit finding efficiency and they were abandoned in favor of sparse pedestals.

The origin of the pedestal shifts is not completely understood but it appears to be related to the readout time difference between sparse data and latch all data. If, for example, radiation damage shortened the hold time constant of the sampling capacitors in the SVXD chips such an effect could appear.

An option existed in the offline analysis to perform also gain corrections on a strip by strip basis. Since gain variations were small in any local region of the detector there was little perceived advantage to doing this and it was omitted. With radiation damage, significant gain differences developed between the inner and outer layers. If pulse height data from the SVX are used in any serious energy loss measurements these corrections can be applied.

14.1.1 Strip Clustering

After pedestal subtraction, the read out strips are clustered. The clustering algorithm begins by grouping contiguous strips. If there exists a known dead strip, it is also included in the grouping. A threshold is then applied to each non–dead strip in the group, where the threshold is based on the measured strip noise and the number of strips in the group. For example, if the group has 5 strips, each strip is required to have charge greater than twice its noise. This factor varies for the number of strips in the cluster (see Table 14.1.1). If a strip fails this requirement or there are contiguous dead strips, the grouping is broken at that strip into two (or more) and the test is done again on each remaining group. Remaining groups are saved as clusters.

Number of Strips	Multiplicative Factor
One	4.0
Two	2.5
Three–Eight	2.0
$\geq$ Nine	1.5

Table 10: Multiplicative factor to set thresholds for various cluster lengths

Cluster positions are calculated as a charge weighted centroid, using individual strip charges and the strip center position. The cluster position error is assigned based on the total charge and the number of strips in the cluster. For clusters with charge $\geq$ 11.7 fc or $\geq$ 4 strips in the cluster, the position error is set to (strip pitch $\times$ number of strips)/$\sqrt{12}$). Remaining clusters use as errors values obtained from a study of the residual distributions

Number of Strips	Assigned Cluster Error
One	15 μm
Two	13 μm
Three	25 μm

Table 11: Cluster errors for clusters with charge $\leq$ 11.7 fc

from the final track fits. We chose a value which gives the normalized residual distribution a width of 1. Table 14.1.1 summarizes the errors used for 1, 2, and 3 hit clusters.

14.1.2 Cluster Charge Distributions

Cluster pulse height distributions are dependent on proper pedestals corrections and track angular distributions. After corrections using sparse pedestals the pulse height distributions were consistent over the detector. In Figure 72a we show a raw pulse height distribution of clusters on tracks. In Figure 72b we show the sample distribution corrected for the track polar and azimuthal angle. Cluster lengths are sensitive to clustering cuts and track angle to the silicon. For the clustering cuts indicated in Table 12 we show the strip multiplicities in Figure 73. These were consistent layer to layer. In Figure 74 we shown the average cluster length versus the angle between the track and the silicon detector normal vector. The observed shift, which is consistent from layer to layer, is close to the Hall angle in these detectors.

14.1.3 Hit Efficiency

The hit efficiency of the SVX ladders depend upon a number of contributions. These include signal to noise ratio, sparse readout, pedestals, clustering, pattern recognition, bad regions, and geometrical acceptance. In calculating hit efficiencies from data we do not separate out the effect of bad regions and geometrical acceptance since these are irreducible for a given barrel. Explicitly, the geometrical acceptance refers to gaps in z between crystals on a ladder, and gaps in ϕ between ladders, in particular on the innermost layer. Because of these effects, and bad regions, we can never have 100% hit efficiency.

Hit efficiency is studied by counting tracks, found by the CTC, which extrapolate into the SVX four layer tracking volume and have missing hits on various layers. Measured hit efficiencies can be strongly dependent upon track quality and pattern recognition. For this reason we cannot really measure hit efficiency in isolation from questions of track efficiency and resolution. For example the hit efficiency can be inflated at the expense of resolution if noise clusters are added to tracks. Measured hit efficiencies have been determined iteratively by applying optimized track quality cuts to the test samples. If this is not done, the hit efficiencies will always be too high. This study has been done for data taken before and after significant radiation exposure.

For early data, where radiation effects are negligible, typical measured efficiencies on the four layers were 93% (Layer 0), 93% (Layer 1), 93% (Layer 2), and 91% (Layer 3). These values include losses due to bad strips and geometrical acceptance. In particular there is a fixed 5% loss on Layer 0 due to azimuthal gaps between ladders. The bad strip fraction changed with time but was typically less than 1% for early running, except for Layer 1

where it was 3% due to a bad SVXD chip. For missed hits we find no raw or unclustered data present within a road defined for the test track about 40% of the time. This implies that part of our inefficiency is due to clustering cuts and the rest to the sparse readout.

For data taken late in the run, the most probable MIP to noise ratio decreased on the innermost layer from 9:1 to 6.5:1. As a consequence, the efficiency on that layer decreased. Typical hit efficiencies on the four layers became 89% (Layer 0), 85% (Layer 1), 91% (Layer 2), and 89% (Layer 3). The bad strip fractions, which are included in these efficiencies, were typically 5–6% on layers 0 and 1 and 1.5–2% on layers 2 and 3 for the later running. Part of the degradation on Layer 1 is due to the surface effects discussed in Section 13.3. Towards the end of the run, the sparse thresholds for the innermost layer were lowered in an attempt to recover efficiency. The fraction of missed hits with no raw (unclustered) data, in the tracking road, decreased on the innermost layer and this is presumably due to additional noise hits within the tracking road.

14.2 Track Finding

Track finding in the SVX makes use of the progressive method [38], which starts from an external fit, in the CTC, and adds points progressively to the track.

14.2.1 Tracking Algorithm

We make use of the following generalized tracking algorithm: Begin with the track fit in the external detector (the CTC). Extrapolate the track parameters to the next measurement plane closer to the interaction vertex, accounting for multiple scattering and ionization energy loss in any material between the two measurement points. This step affects both the track parameters and track error matrix. Define a road, based on the intersection point and the track error matrix, to look for clusters to add to the track fit. For each cluster, define a track candidate by adding the cluster to the existing fit. Extrapolate each candidate to the next measurement plane and continue. This procedure is iterated until all measurements along the track are included.

This method has several advantages over a global track fit in the two detectors:

- We can use the external track parameters to drive the pattern recognition part of the track finding algorithm.
- The method updates the track χ^2 at each step, so it can be used to pick the best of several possible track candidates associated with an external track.
- It is an efficient use of CPU cycles, since it requires the inversion of 2 matrices of order the number of track parameters (in general, there are 5 parameters to define a track) for each point added.
- Alignment corrections can be included at each step of adding a new point to the existing fit.

Once all measurement planes have been included, track selection is done. Track candidates are required to have clusters from two different layers added to the fit. We choose the track candidate based on the number of associated clusters and candidate χ^2 below an absolute cut. The first choice is the candidate with lowest χ^2 from candidates with 4 associated clusters, then the candidate with the lowest χ^2 with 3 associated clusters, then the candidate with the lowest χ^2 with 2 associated clusters.

14.2.2 Track Finding Efficiency

We study our track finding efficiency by starting with well reconstructed CTC tracks which extrapolate within the SVX fiducial volume. By requiring that the track pass through two or more layers of the SVX detector, we can calculate a measured tracking efficiency given a track finding and reconstruction algorithm. For the current tracking algorithm and alignment constants, we measure an efficiency of 98% for runs before significant radiation damage occurred. Of these found tracks, 70.5% have 4 associated clusters, 23.0% have 3 associated clusters, and 4.5% have 2 associated clusters. These numbers can be compared with expectations based upon the single layer hit efficiencies which predict 73.2% with 4 associated clusters and 24% to have 3 associated cluster. Differences can be due to correlations in bad regions from layer to layer.

For data taken near the end of the run, radiation damage decreases the tracking efficiency. At that time we measure a total efficiency of 97%. Of these found tracks, 58.1% have 4 associated clusters, 30.6% have 3 associated clusters, and 8.6% have 2 associated clusters. Single layer hit efficiencies predict 61% 4 hit tracks and 32% 3 hit tracks. Typical uncertainties on these numbers are 1–2% due to the statistics of the tracking samples used.

14.2.3 Resolution

As discussed in Section 3.3, the expected SVX resolution is based upon the geometry and composition of the detector. The actual performance will be degraded further due to misalignment, miscalibration, pattern recognition errors, and uncertainty in the location and total amount of material in the detector. In Figure 75, we show the measured impact parameter resolution versus transverse momentum from data taken early in the run. In this plot, the asymptotic value at high p_t is dominated by the size of the Tevatron beam spot. By reconstructing the primary vertex using multi–track events we can measure the convolution of the true beam spot size with residual misalignments and other degrading effects. This convolution is found to be Gaussian–like with a sigma of 35–36 μm. In Section 15.3.3 we discuss the wedge–to–wedge misalignments, but they are found to be distributed with an RMS of 12 μm and consequently do not dominate the spot size determination.

In Figure 76, we show the impact parameter resolution (not including the contribution from the primary vertex error) versus the track momentum, for tracks with 4 associated clusters. This plot is obtained by subtracting off the beam spot size in quadrature leaving in the wedge–to–wedge misalignment. The asymptotic value at high p_t is now in principle related more directly to the intrinsic resolution of the SVX. However, since all the data used in the fit is at fairly low p_t, the asymptote is not necessarily unbiased. This plot may be considered a good representation of the resolution of the SVX in the region of p_t occupied by many of the tracks from B decay and B decay products. Estimations of the SVX resolution at high p_t are discussed further in Section 15.3.3.

In Figure 77 we show the improvement in the reconstructed ψ mass for decays into muons when the SVX is included in the track fit.

15 Alignment

15.1 Alignment using Track Data

The optical survey data discussed in Section 10.3 is used as a first estimate on silicon detector positions within the SVX. The device is realigned in place using track data. Given the large

number of components in the SVX, the process is rendered tractable by decomposition into set of steps which isolate the more significant degrees of freedom.

Since the SVX tracking is highly coupled to the CTC tracking, the alignment procedure has also to prevent any possible CTC systematic effect from propagating significantly into the SVX alignment constants.

The offline alignment procedure has been decomposed into a set of steps. The global alignment consists of aligning each barrel (treated as a rigid body) to the CTC. The wedge internal alignment consists of alignment of the individual ladders (treated as rigid bodies within a wedge). The wedge–to–wedge alignment consists of the relative alignment of the wedges within a barrel. We know that the 3 individual silicon crystals within each ladder are aligned during construction to within 5 μm, and we therefore do not attempt to use tracks to correct for possible misalignment inside ladders. The overall offline alignment process is iterated to convergence.

15.1.1 Global Alignment Procedure

The method relies on the fact that the CTC and any SVX barrel should see the beam line at the same location for a given run. The global alignment is adequate as long as its accuracy is much better than the resolution of the extrapolated CTC track. The relative alignment of the two barrels needs to be done to a precision set by the scale of the SVX resolution. The global alignment procedure is the step where most of the effect of possible CTC systematics is concentrated.

Each SVX barrel is treated as a rigid body with 6 degrees of freedom (or alignment parameters), corresponding to 3 rotations (around the x, y, and z axes) and 3 translations (along the x, y, and z axes). Only 5 of these alignment parameters are refined using tracks since the SVX provides only measurements in the $x - y$ plane. For the last alignment parameter, which is the z position of the barrel, we rely on the survey measurement.

The beam line is measured twice with the same sample of events from a common run. First, good CTC tracks with $p_t > 1$ GeV/c are used to measure the beam line as seen by the CTC. Then, good CTC tracks that have 4 good SVX hits in the considered barrel are refitted including the SVX information and used to measure the beam line as seen by the SVX barrel. The difference between the two measurements determines the corrections to the x and y translations and the x and y rotations of the barrel with respect to the CTC.

The rotation around z is determined by optimizing the match between the CTC track extrapolations to the SVX and the location of the corresponding SVX hits.

Global alignment constants determined with tracks have typical statistical uncertainties of 5 μm for translations and 0.1 $mrad$ for rotations. The differences between the optical installation survey constants and the offline alignment constants are compatible with the error on the survey measurement. However, the final constants have an error much smaller than the survey measurement error.

15.1.2 Wedge internal alignment procedure

The wedge internal alignment consists of finding the relative positions of the ladders within each wedge. This is done using good CTC tracks having 4 good SVX hits in the same wedge and a p_t above 3.5 GeV/c.

The SVX alone is able to measure 3 track parameters, namely the impact parameter d_0, the azimuthal angle ϕ_0, and the half curvature c. However, the accuracy of the SVX alone to

measure the curvature is limited due to the small lever arm. The CTC measures all 5 track parameters; however, in order to avoid a strong propagation of any possible CTC systematic effect into the internal alignment constants, the only CTC information that we want to use in the internal alignment procedure is the information that the SVX itself cannot provide. Therefore, each selected track is refitted through the SVX hits, keeping fixed the values of the parameters $\cot\theta$, c, and z_0, determined by the CTC, and ignoring the rest of the CTC information.

For the alignment procedure itself, each selected track is constrained to pass through the average beam line (previously measured as explained in Section 15.1.1) and its SVX hit on the outermost ladder. With the CTC information on $\cot\theta$, c and z_0, this completely determines the track in 3 dimensions. The quantity Δx is computed for each of the 3 inner ladders; Δx is the distance (in the local coordinate x) between the track intersection with the ladder and the cluster position. Each of the 3 innermost ladders is allowed to float with respect to the outermost ladder, and its position is determined by minimizing simultaneously the quantities Δx of all the selected tracks at that particular ladder.

Each of the floating ladders, treated as a rigid body, has the 5 following alignment parameters (note that the translation along the z axis is not considered here, i.e. we assume that there is no shift in z between ladders of the same wedge):

- a translation perpendicular to the strips in the plane of the silicon
- a rotation in the plane of the silicon
- a translation perpendicular to the silicon plane (radial shift)
- a rotation around an axis parallel to the strips
- a rotation around an axis perpendicular to the strips and parallel to the silicon plane

To first order, the first two of the above parameters affect the azimuthal ϕ position of the clusters, whereas the last three affect the radial position of the clusters.

The result of this fitting process indicated that residuals on the three floating layers were minimized only when systematic radial shifts in the ladder positions were introduced. In the SVX, layers 0 and 3 face inwards towards the beamline (strip side) while layers 1 and 2 face outwards. The preferred radial shifts were always in the direction of the electric field within the silicon. In some cases these radial shifts were as large as 200 μm. Comparisons to optical data are discussed in Section 15.2 below.

Figure 78 shows the χ^2 distribution of all these tracks, before any track alignment and after alignment allowing radial shifts. As expected, the track χ^2 is improved on average by the alignment procedure. The residual distribution for all tracks in all wedges is shown in Figure 79, before and after alignment. For each track, the 4 residuals obtained by fitting the track through the 4 SVX hits are entered in the distribution. The width of this distribution (sigma from a Gaussian fit) goes from 17.6 μm down to 10.6 μm after track alignment. A simple Monte Carlo program then is used to determine the average spatial resolution at the silicon from the mean residuals. At this level of alignment, the resolution is found to be around 13 μm. The corresponding impact parameter resolution for high p_t tracks is consequently also close to 13 μm.

15.1.3 Wedge–to–wedge alignment

The wedge internal alignment procedure does not correct the internal alignment parameters that were derived for the layer 3 ladders from the optical survey measurements. Therefore,

Layer number	Overlap in nominal geometry	
	$\Delta\varphi$ angle	Number of strips
3	0.04°	~ 1
2	0.30°	~ 4
1	0.32°	~ 4
0	−1.26°	gap !

Table 12: Azimuthal overlaps of two adjacent wedges

after the wedge internal alignment, the misalignment between layer 3 ladders become misalignments between wedges.

The method that has the most statistical power to determine the relative wedge alignment is probably to use tracks that cross regions of the SVX where two identical ladders in adjacent wedges overlap in φ. The difficulty is that the acceptance of these overlaps is very small (see Table 12). This type of alignment needs therefore a lot more statistics than the other ones and has not been done as yet.

The effect of the misalignment from wedge to wedge on the wedge average impact parameter has been determined from the $W \rightarrow e\nu$ and the inclusive electron samples. These results were used to evaluate the systematic uncertainty on the inclusive B lifetime measurement due to wedge–to–wedge misalignment.

15.2 Comparison of optical and tracking alignment constants

It is important to determine whether alignment constants determined from tracking data correspond to real physical displacements of the detector elements. Non–physical components in the alignment parameters can arise from at least two sources: uncorrected systematic effects and strong couplings between two or more parameters in the alignment algorithm. The Hall effect, non–linearity in the readout electronics, the effect of charge carrier diffusion and non–ideal ladder geometry all represent potential sources of systematic bias, and could all contribute to apparent, non–physical displacements of the detector. In many cases, such shifts simply correct for the systematic error and have no adverse consequences on detector performance. Coupling between alignment parameters, however, could, in principle, introduce large non–physical distortions to the overall geometry and may produce corresponding systematic errors in vertexing and impact parameter measurements. Such couplings could be driven by residual misalignment in parameters not included in a fit. In this section, we will attempt to address the question of nonphysical displacements.

To test the stability of the algorithm and the coupling between various constants, we compare the results of fits for only two parameters with those of fits for three. If the constants are not strongly coupled, then the two parameters of the first fit should not change significantly when the third parameter is allowed to float. While some differences are seen which are larger than the estimated errors, the absolute magnitude of the shifts are small enough to be ignored in any application of the SVX.

Direct comparison of optical survey constants and those derived from track alignment only show significant shifts for the ladder radial positions. Figure 80 shows the radial shifts as a function of wedge and layer number. Some ladders appear to have moved by 200 μm or more, compared to estimated statistical uncertainties in the range 6–8 μm. Notably, both

barrels exhibit the same pattern of displacements by layer: Layer 0 moved inward, while Layers 1 and 2 moved outward. Although no clear pattern in azimuth emerges, there exists a strong correlation for the ladders within a given wedge.

Given the clear systematic correlation of these shifts with layer number we believe that the effect cannot be due to some geometrical misalignment or accidental shift occurring after construction.

One possibility is that charge transport properties of the silicon itself may induce an apparent shift in the effective measurement plane away from its assumed position at the center of the silicon. Diffusion, for instance, is known to produce this type of effect but the magnitude here is too large. If the shift were due to an effect in the silicon, then one might suppose that a single parameter, δ, describing the distance of the effective measurement plane from the center of the detector could explain all of the radial shifts:

$$r_i^{eff} = \begin{cases} r_i^{true} - \delta(1 - \frac{r_i^{true}}{r_3^{true}}) & \text{for } i = 0 \\ r_i^{true} + \delta(1 + \frac{r_i^{true}}{r_3^{true}}) & \text{for } i = 1,2 \end{cases} \tag{19}$$

where r_i^{eff} and r_i^{true} are the effective and actual layer radii, respectively, and $\delta > 0$ implies a shift toward the strip side of the detectors. In addition, we assume that $\delta \ll r_i^{eff}, r_i^{true}$, and that Layer 3 is fixed at r_3^{true}. A positive value of δ (consistent with diffusion, for instance) then yields the sign of the radial shifts observed in the data.

Table 13 shows the values of the constant δ inferred by the radial shifts on each layer. Assuming that the width of the difference distribution plotted in Figure 80, about 20–30 μm, sets the scale of the overall uncertainties in the radial position measurements, then the listed values of δ are roughly consistent with a 70 μm shift in the effective measurement plane. Since 20–30 μm is likely to be an over–estimate of the uncertainty in radial survey, this conclusion is probably somewhat optimistic.

Table 13: The value of δ for each layer. Radial shifts have been averaged over both barrels.

Layer	Mean shift (μm)	r_i/r_3	δ (μm)
0	50	0.62	81
1	-80	1.54	52
2	-147	1.72	85
Average δ:			73

The origin of the radial shifts is thus not understood. We choose therefore, to assign a systematic uncertainty of 100 μm to the radial position of the SVX ladders. We can evaluate the effect such radial displacements could have on a lifetime measurement. In the worst case, a radial shift would translate directly into a scale factor on the secondary vertex position and thus on the measurement of the lifetime $c\tau$. The deviation of this scale factor from unity will depend on the ratio of the ladder displacement to the nominal radius of the ladder. We thus find that a 100 μm displacement corresponds to a systematic uncertainty on $c\tau$ of

$$\frac{\delta(c\tau)}{c\tau} = \frac{\delta r}{r} = \frac{100\ \mu\text{m}}{3\ \text{cm}} = 0.3\%$$

This systematic uncertainty must be included in all lifetime measurements until the radial shifts are better understood.

15.3 Checks of Alignment

The alignment procedure described in the previous chapter used jet data from a single run to determine the global and internal alignment constants. In this section we present a number of distributions that test the quality of this alignment.

15.3.1 Alignment relative to CTC

Because the SVX resolution is so much better than that of the CTC, the SVX essentially determines the impact parameter and azimuth of the track. Global alignment of the SVX to the CTC therefore effect lifetime measurements only to second order. However to use the increased lever arm of the SVX to improve momentum measurements the relative alignment of the CTC and SVX must be well understood.

As a check of the global alignment, we have studied the impact parameter distribution of inclusive $e^{\pm}$ ($p_t > 10$ GeV/c) using the beam positions determined from the SVX but using CTC information alone in the $e^{\pm}$ track fit. These data indicate a global offset of 29$\pm$ 8 μm for e^+ and 49$\pm$ 8 μm for e^- respectively.

We have also determined the average beam position in W decay events both from CTC and CTC+SVX fits. Here the CTC and SVX beam spots to differ by -4 ± 3 μm in x and -5 ± 3 μm in y. Based on these data we believe there is at most $\sim$ 40 μm systematic uncertainty on the relative alignment of the SVX and the CTC. This uncertainty is a small fraction of the present CTC resolution on the impact parameter, which is $\sim$450 μm. Such a bias has negligible effect on low p_t tracks which are the bulk of B decay products.

15.3.2 Relative Alignment of the Two Barrels

To check the internal consistency of the global alignment and search for time dependent alignment problems we separately fit the beam position using tracks from each barrel. The results of these fits are compared and the barrel–to–barrel misalignment is calculated run by run. The bottom plot of Figure 81 shows for a single run the x beam positions as obtained from barrel 0 (triangles) and barrel 1 (circles) as a function of z. The two lines are the results of independent straight lines fits to the data for each barrel . The figure clearly demonstrates that the two barrels are aligned to much better than the single event vertex resolution. Each beam line is characterized by two offsets, x_0 and y_0 and two slopes s_x and s_y. The differences in x_0 and y_0 between the two beam lines are shown on Figure 82 as a function of run number over a few months. Corresponding plots for s_x and s_y are shown on Figure 83. Using such data we estimate a maximum misalignment between the barrels of $\pm$10 μm in x and in y. There is no evidence for systematic shifts as a function of time.

15.3.3 Internal Alignment

Measurements of the SVX internal alignment are not strongly coupled to CTC tracking. Checks of the internal alignment utilize the two track parameters well measured in the SVX, the impact parameter (with respect to the beam position) and the azimuthal angle.

A number of data sets are used to check either resolution or systematic effects. Electrons from W decay are prompt and free of multiple scattering effects but are a small sample. Inclusive electrons have a broad impact parameter distribution but provide a large sample for systematic offset checks. Back to back muons from Z decay are another small sample but provide a clean measurement of asymptotic resolution.

Figure 84 shows the residual distributions for SVX layers 0 through 3 using electrons from W decay. The residuals are calculated with respect to the combined CTC–SVX fit without removing the selected SVX layer from the fit. Gaussian fits to these distributions indicate that the mean residuals for all four layers are centered at zero to within ± 3 μm, and that the sigma is between 13.5 and 16.5 μm depending on the layer number. We note, however, that distributions have significant non–gaussian tails. These data exhibit a resolution which is higher than the average resolution of 10 μm derived from the results of the wedge internal alignment. This is not a surprise because the resolution is measured here with tracks fitted using both CTC and SVX information. Even with perfect CTC alignment, we would expect the residuals of the combined fit to be larger than for the SVX only fit, since CTC resolution errors will pull the fitted parameters. In addition, the resolution is also expected to be degraded by wedge–to–wedge misalignment. Such misalignments are also a possible source of non–gaussian tails in the resolution function.

The inclusive electron data are well suited to study wedge–to–wedge deviations in response. Figure 85a and b show the distribution of impact parameter for $e^{\pm}$ while Figure 85c and d show the mean value of the impact parameter as a function of wedge number. A $p_t > 10$ GeV/c cut has been applied. As in the W analysis, the impact parameter is determined from a combined CTC–SVX fit and the SVX beam position. The fitted value d_0 is therefore primarily determined from SVX information. Deviations of ~ 20 μm are visible and the RMS is about 12 μm. The size of the effect is independent of the charge of the $e^{\pm}$. We believe these deviations result from misalignment between the SVX wedges.

Because the beam spot is ~ 36 μm, we are unable to use the W or inclusive electron samples to verify the impact parameter resolution of the SVX, σ_{d_0}. We have checked σ_{d_0} by studying the $Z \rightarrow \mu^+\mu^-$ decays, where the two muons are nearly back–to–back in the transverse plane. The method is to measure the sum of the signed impact parameters of the two leptons. We have further checked this result using a small sample of Dalitz decays, where this time we compute the difference of the signed impact parameters of the two leptons (because they are parallel rather than antiparallel as in the Z case).

Figure 86 shows the distribution of the sum of the impact parameters of the Z legs. A Gaussian fit to this distribution shows a sigma of 24 μm, from which we derive:

$$\sigma_{d_0} = 24/\sqrt{2} = 17\ \mu m$$

This is somewhat higher than the 13 μm resolution expected for high p_t tracks from the results of the wedge internal alignment (Section 15.1.2). The difference in quadrature, 11 μm, could be explained by wedge–to–wedge misalignment and is of the right order for this. The distribution of the sum of the impact parameters divided by the calculated error, also shown on Figure 86, has a fitted sigma of 1.2; this number is compatible with the ratio (measured resolution)/(expected resolution) = 17/13. indicating that our calculated error would be correct if the wedges were perfectly aligned. The 17 μm result is also higher than the constant term in the fit of Figure 76 and in that case the wedge–to–wedge misalignment is included. As noted earlier, that fit is biased by the use of low p_t data and should be considered a valid representation only in the lower p_t region.

15.4 Summary of Alignment

The combined SVX–CTC fits show systematic azimuthal variations on order 12 μm. The mean impact parameter, averaged over azimuth, is centered to better than 7 μm. With current alignment constants, χ^2 and residual distributions in the SVX are well behaved.

The spatial hit resolution derived from these distributions is 13 μm. The operational impact parameter resolution at high p_t is 17 μm due to the added effect of wedge-to-wedge misalignment. The global alignment of the SVX with respect to the CTC is correct to $\sim$ 40 μm. This misalignment has no significant effect on impact parameter or decay length distributions. The effect on $J\psi$ mass or p_t resolution is also negligible, although a small systematic bias may be present for high p_t lepton tracks.

The main mystery remaining in the SVX alignment is the presence of apparent shifts of $\sim$100 μm in the radial position of the SVX ladders. We have been unable to explain these shifts to date. At the present time, we consider this 100 μm shift to be our systematic uncertainty in the radial alignment. This shift corresponds to roughly a 0.3% systematic uncertainty in the overall scale of lifetime measurements.

16 Conclusions

While silicon microstrip detectors have been used successfully in both electron–positron colliders and in fixed target geometry hadron beam experiments, their application to hadron colliders was treated with some initial skepticism. The work described in this paper shows that a complex silicon strip detector system can be operated reliably and within design specification in a hadron collider. The CDF SVX is the first such system to operate in a physics data taking mode.

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64 Average strip leakage on each SVX layer versus integrated luminosity during the run. Period of about 1 year. Leakage current is plotted as a negative quantity. . . . . .

65 Average normalized gain of SVXD chips on each layer of the detector versus integrated luminosity. . . . . .

66 Average normalized noise per channel on each layer of the detector versus integrated luminosity. . . . . .

67 Inferred dose based upon changes in noise, and gain. . . . . .

68 Observed increase in leakage current at layer 0 versus the dose at layer 0 derived from observed noise increase in SVXD readout chip. Note that chip and detector are in principle sensitive to different radiation components and spectra. . . . . .

69 Predicted efficiency loss due to increase in noise. . . . . .

70 Leakage current versus strip number for a wedge which includes a ladder showing anomalous high currents. The leakage current is a positive going quantity here. . . . . .

71 Long term behavior of total bias current on one ladder which is left on continuously. Upper curve shows Tevatron Collider luminosity for many stores.

72 Pulse height distributions for clusters on tracks, a) no correction for polar or azimuthal angle of incidence, b) corrected to normal incidence. Distributions are for Layer 3 detectors. . . . . .

73 Strip multiplicity distribution for clusters on tracks. . . . . .

74 Average cluster length versus incident angle of track with respect to detector surface normal vector. The observed shift is consistent with the Hall angle in these silicon detectors. . . . . .

75 Measured impact parameter resolution of the SVX versus track p_t including the effect of finite beam spot size . . . . . .

76 Measured impact parameter resolution of the SVX versus track p_t corrected for finite beam spot size, pre–radiation damage, 4 hit tracks only . . . . . .

77 Comparison of mass resolution for J/ψ decaying into muons without and with SVX information used in the fit. . . . . .

78 Track fit χ^2 before and after internal alignment corrections, ...

79 Residuals between fitted tracks and measured hits before and after full internal alignment corrections (including radial shifts). Each track contributes four entries to the histogram, one per layer. All four residuals are included in the track fit. Curves shown are gaussian fits. . . . . .

80 Radial shifts for ladders on each layer of each wedge as determined from internal alignment procedure. . . . . .

81 Determination of the SVX global alignment. Bottom plot is x vertex position versus z vertex position of the primary interaction vertices reconstructed with tracks in barrel 0 (triangles) and with tracks in barrel 1 (circles). Units are cm. on both axes and each point comes from a different event. All events are from the same run. The dashed and dotted lines are straight line fits to the triangles and circles respectively. Top plots show beam profile in plane perpendicular to beam line; units are μm. . . . . .

82 Mean horizontal and vertical beam position measured for each run over a 4.5 month period. . . . . .

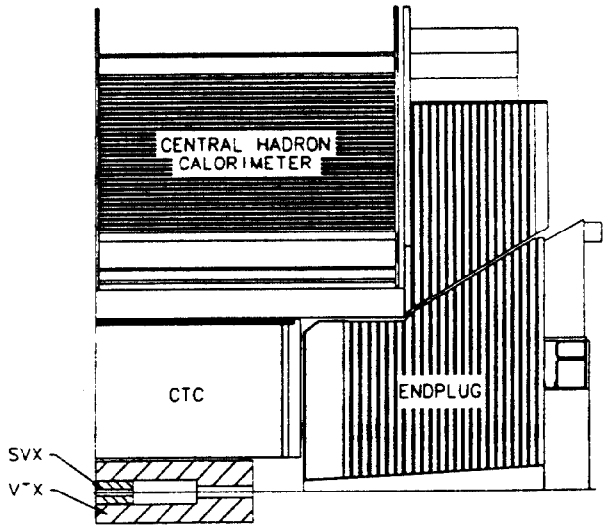
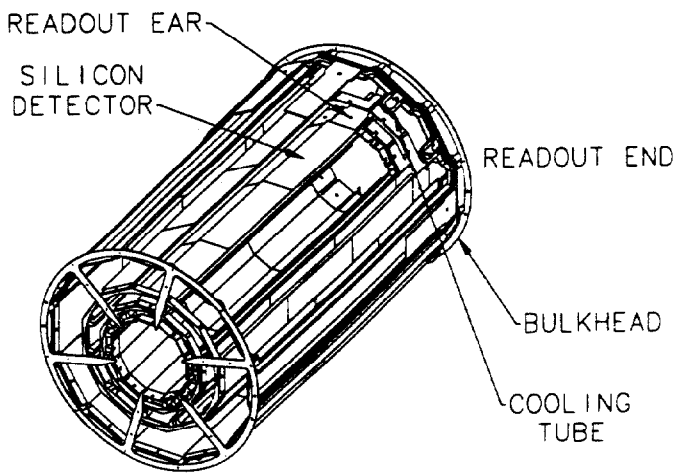


Figure 1



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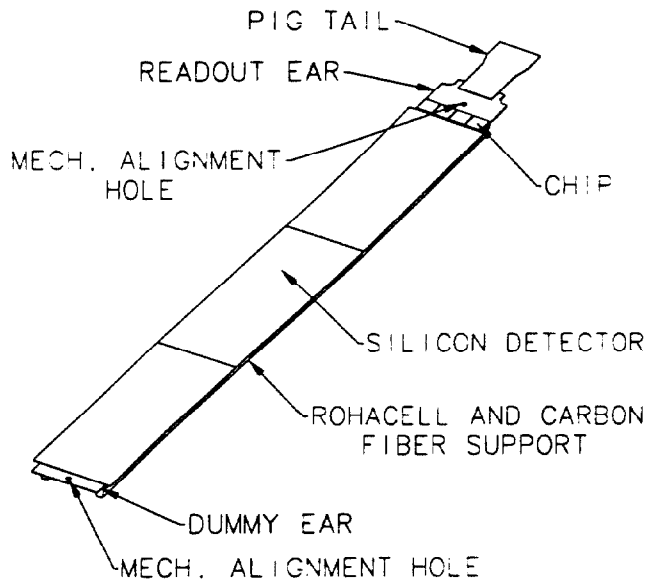

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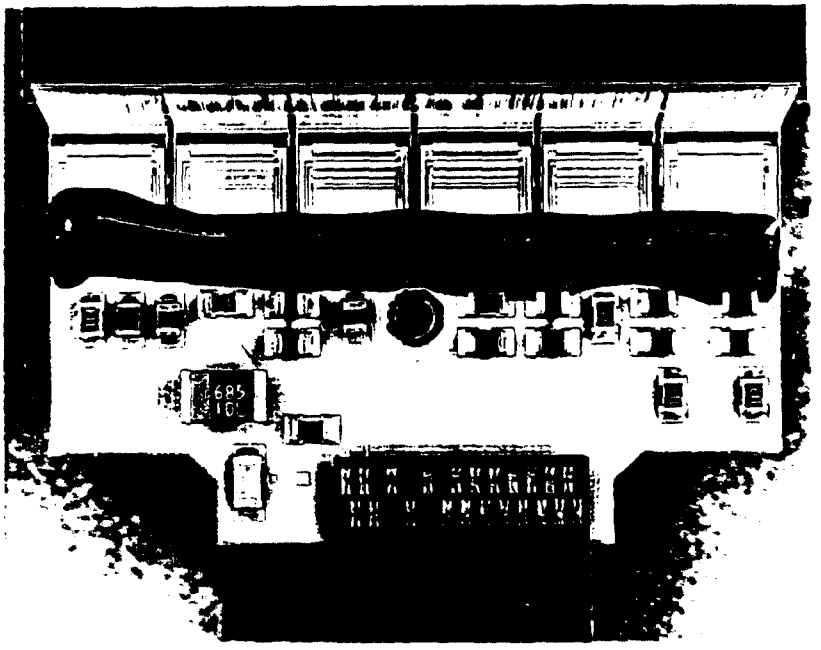

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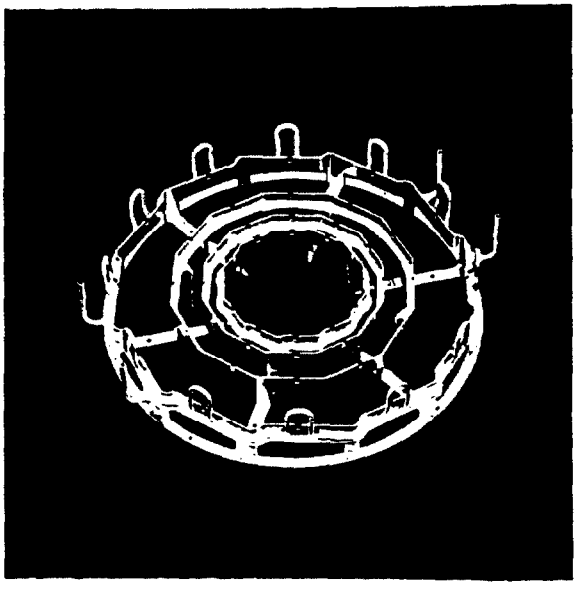

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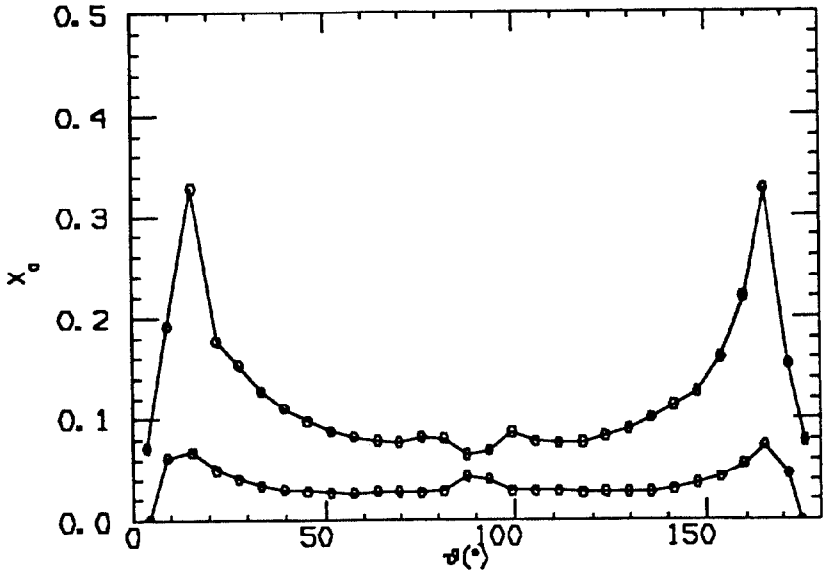

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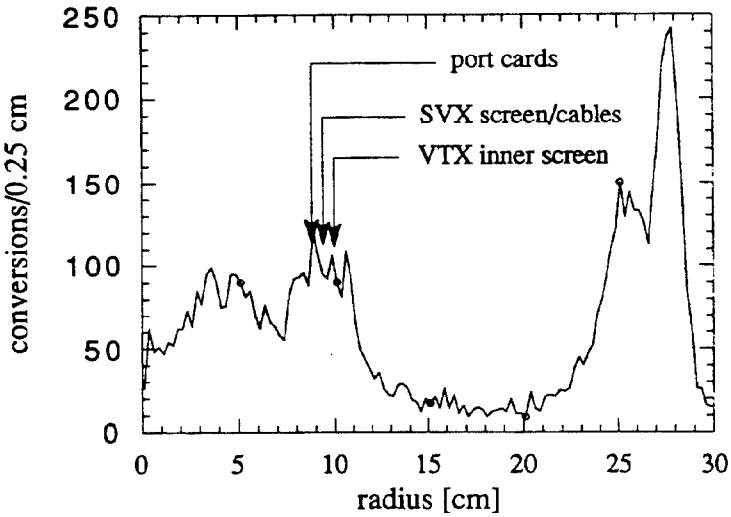

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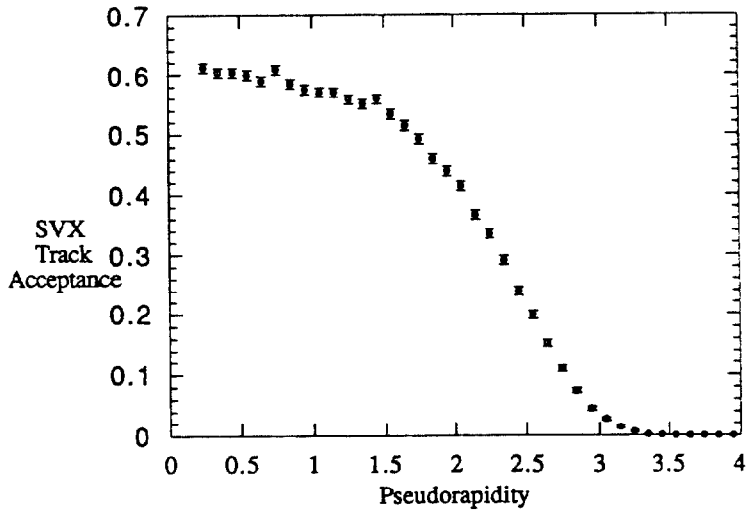

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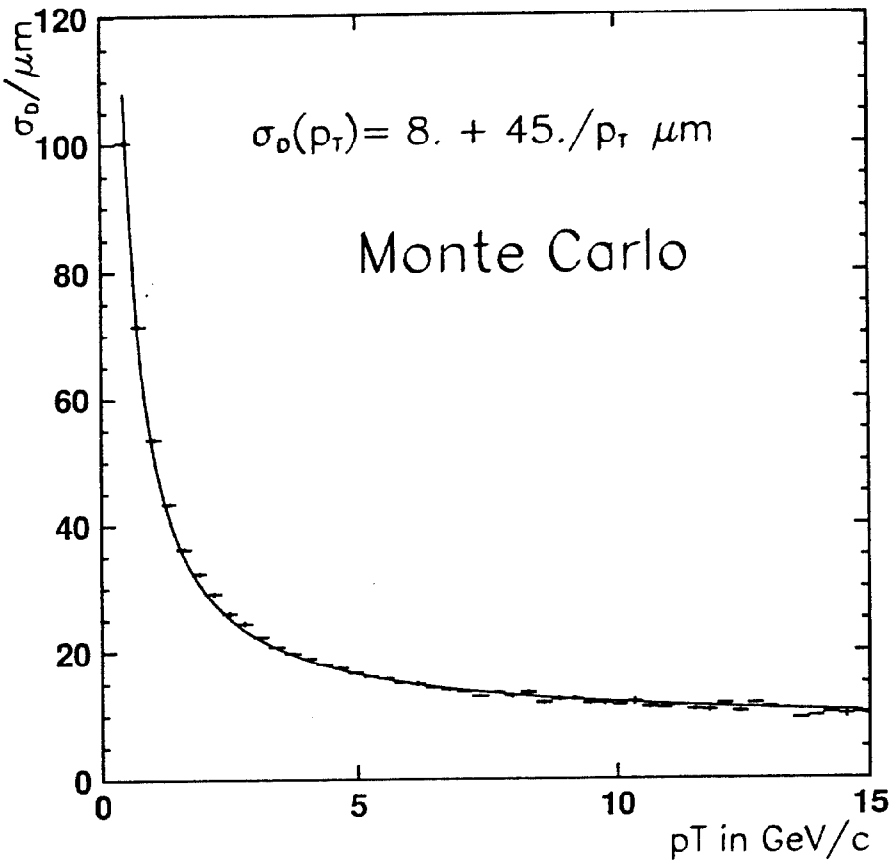

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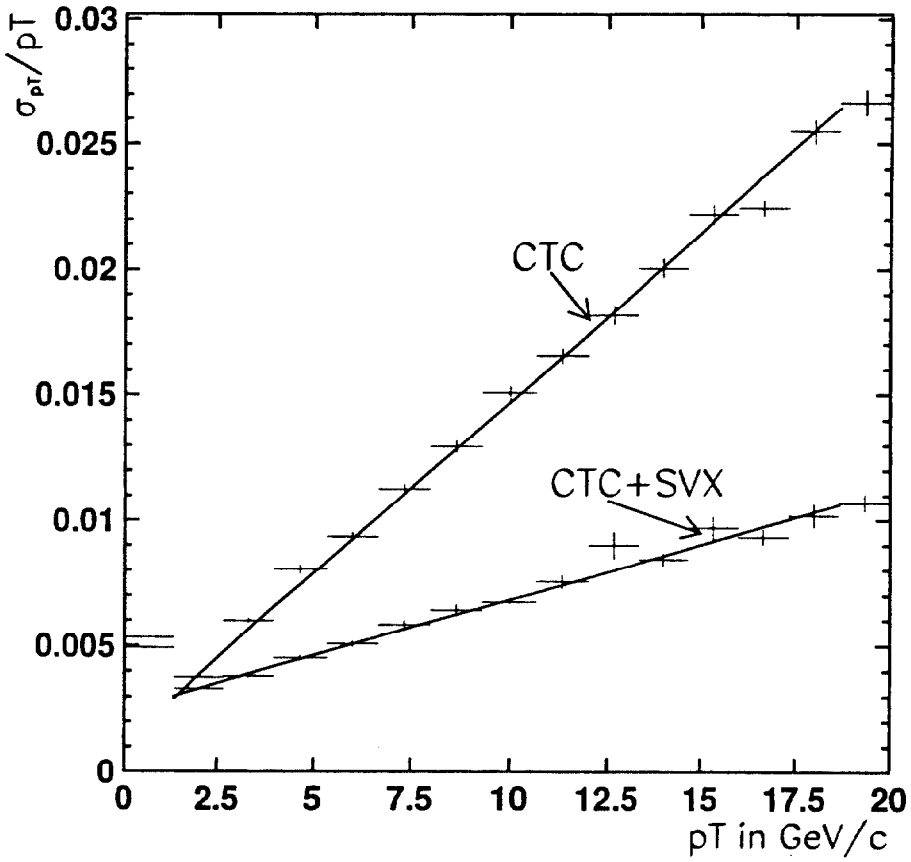

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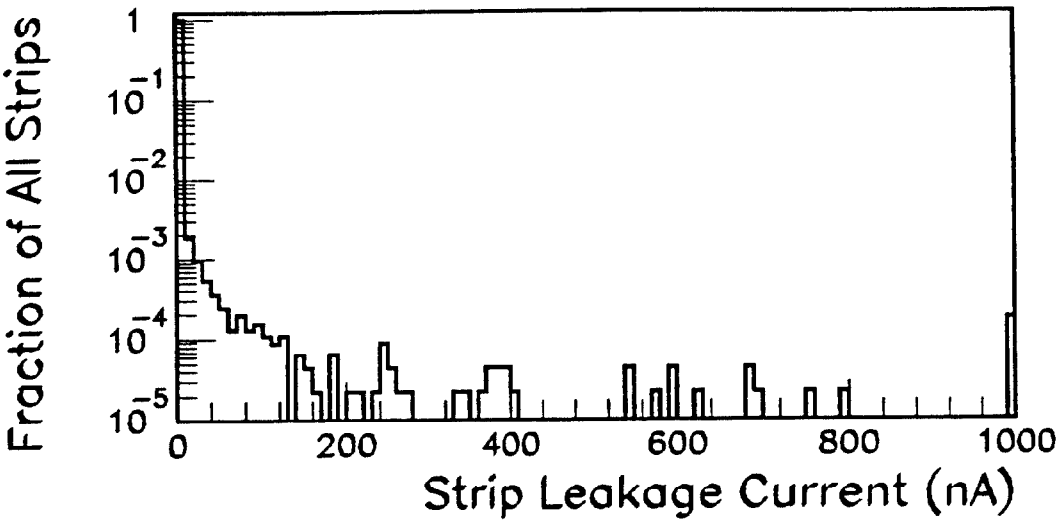


Figure 11a

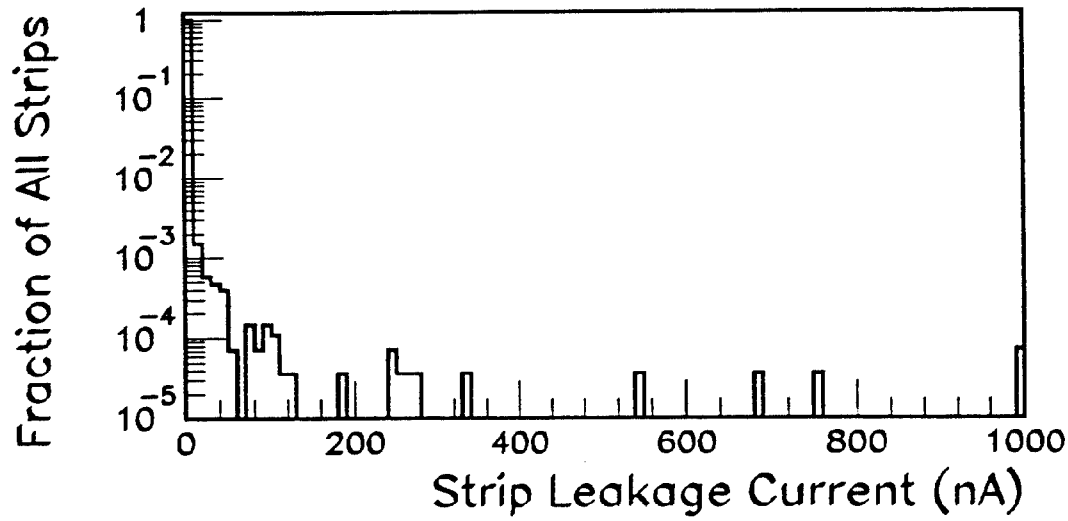
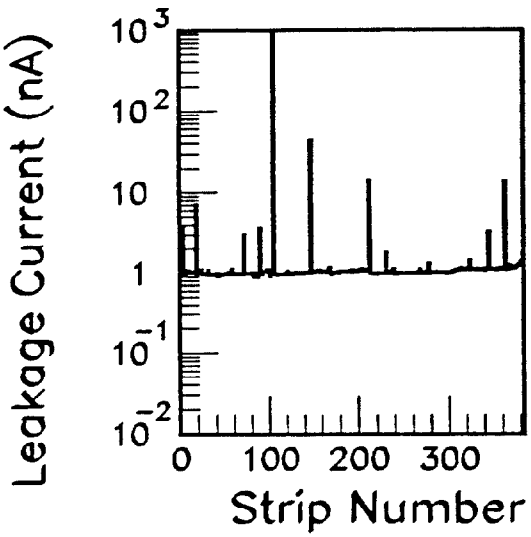


Figure 11b



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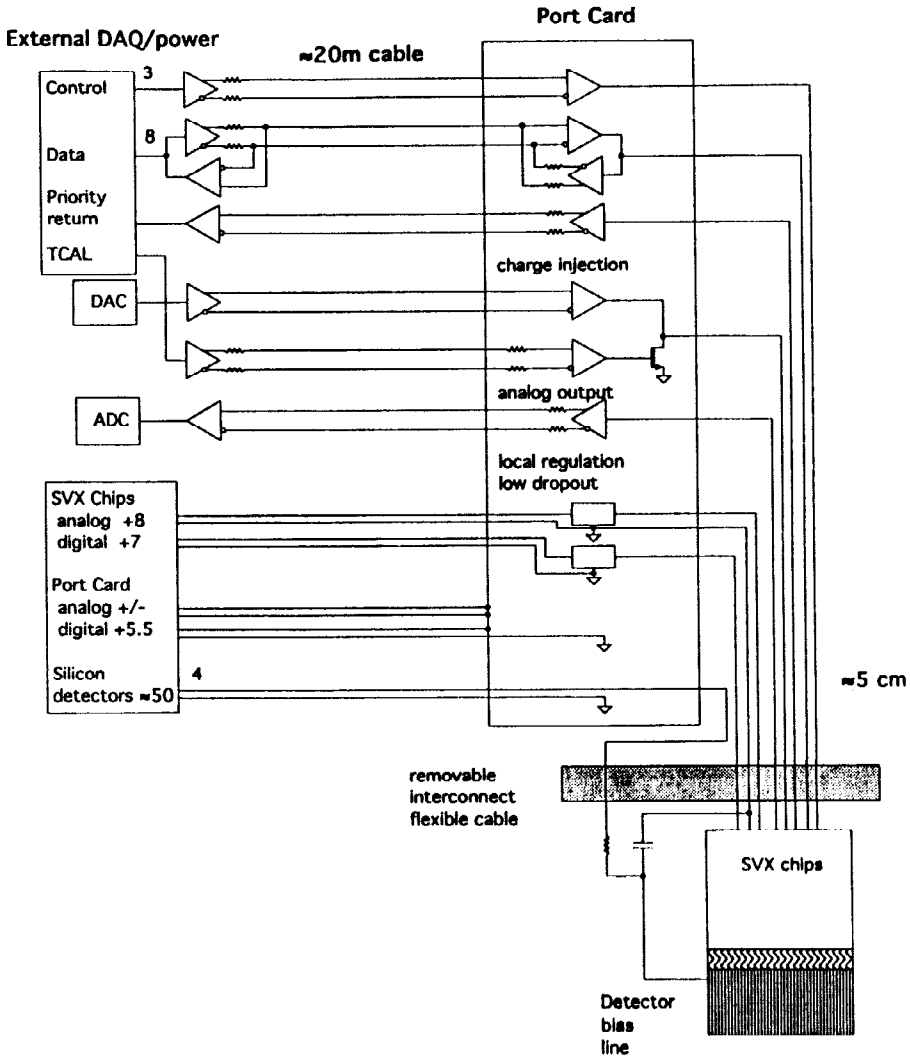

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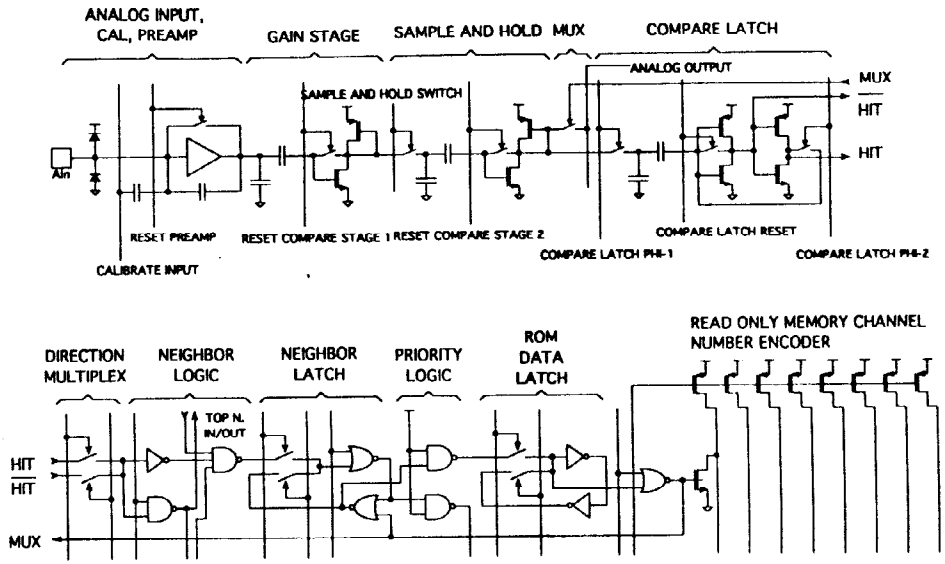

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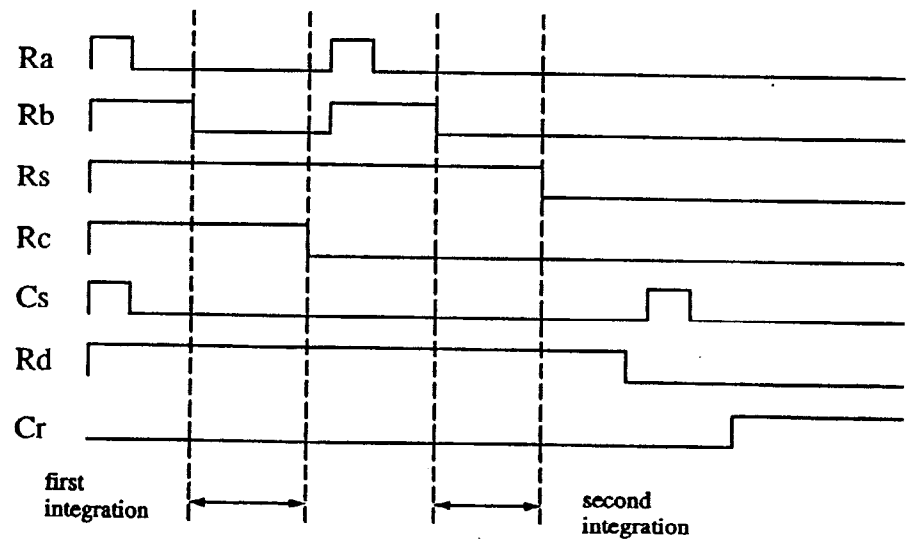

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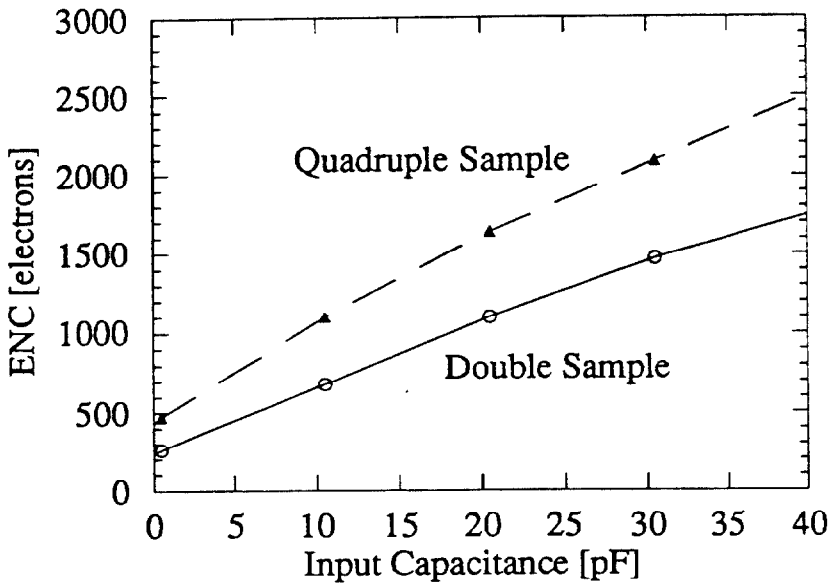

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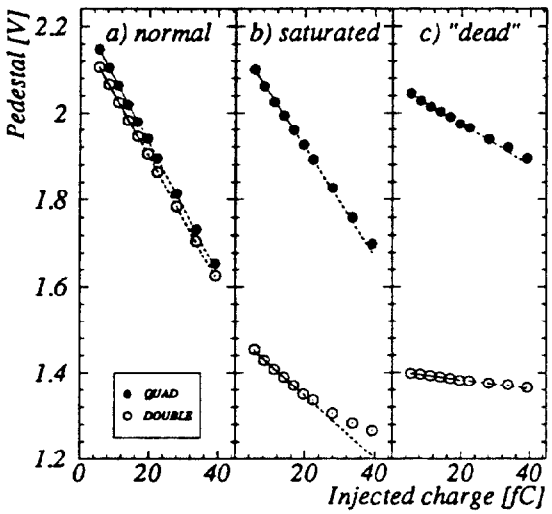

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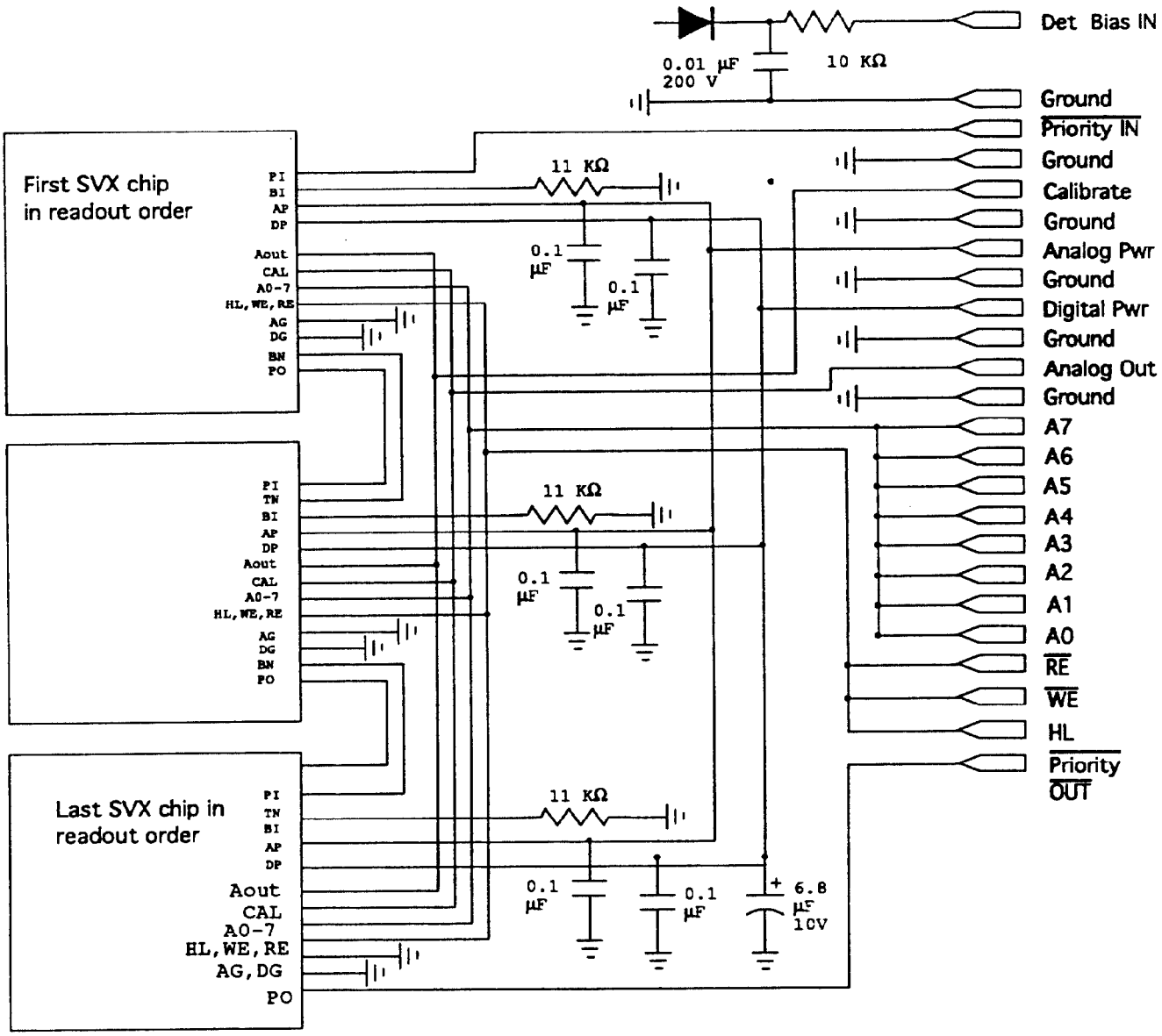
Det Bias IN
0.01 µF
200 V
10 KΩ
Ground
Priority IN
Ground
Calibrate
Ground
Analog Pwr
Ground
Digital Pwr
Ground
Analog Out
Ground
A7
A6
A5
A4
A3
A2
A1
A0
RE
WE
HL
Priority OUT
First SVX chip in readout order
PI
BI
AP
DP
Aout
CAL
A0-7
HL, WE, RE
AG
DG
BN
PO
11 KΩ
0.1 µF
0.1 µF
PI
TN
BI
AP
DP
Aout
CAL
A0-7
HL, WE, RE
AG
DG
BN
PO
11 KΩ
0.1 µF
0.1 µF
Last SVX chip in readout order
PI
TN
BI
AP
DP
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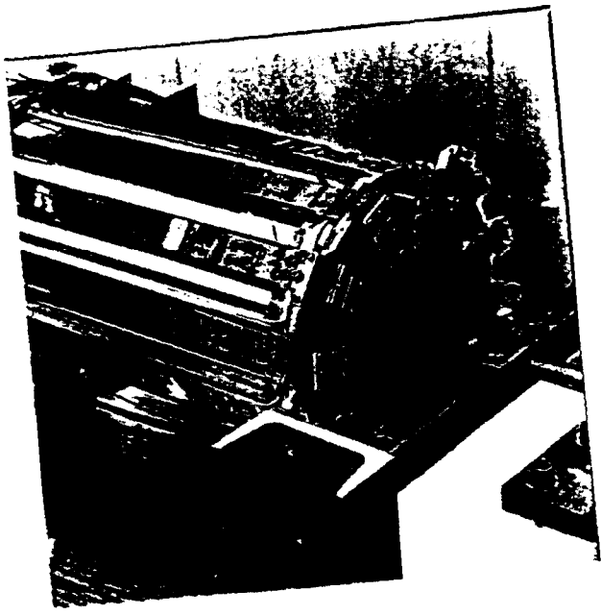
AG, DG
PO
11 KΩ
0.1 µF
0.1 µF
6.8 µF 10V

Figure 18



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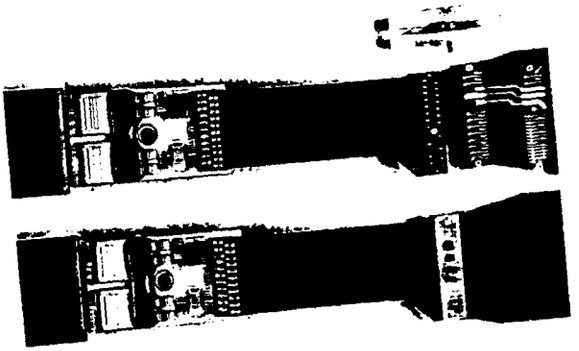

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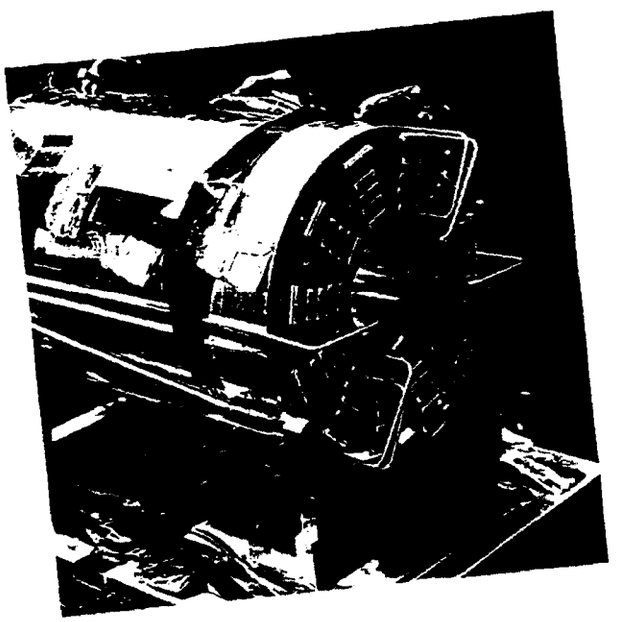

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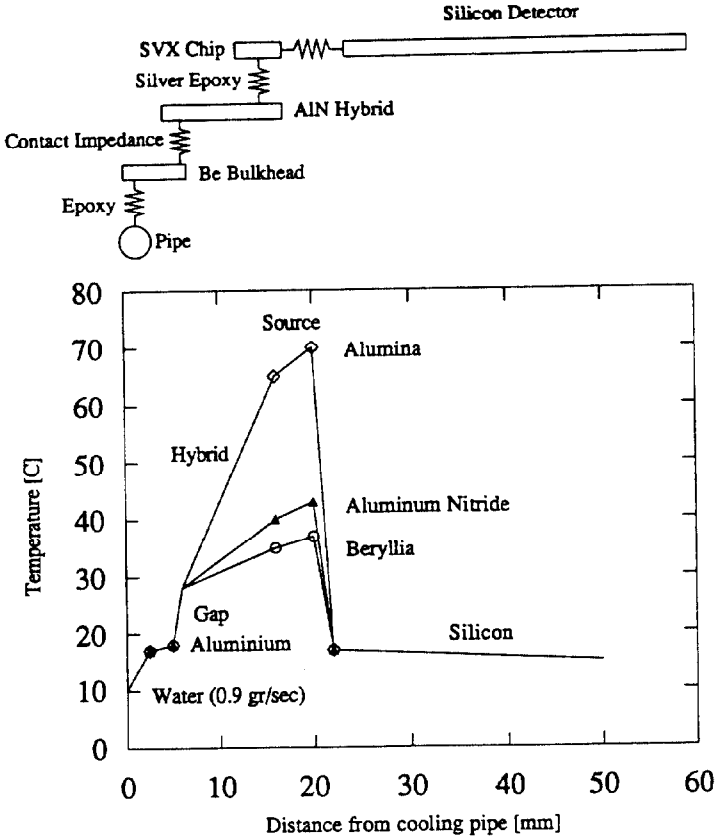
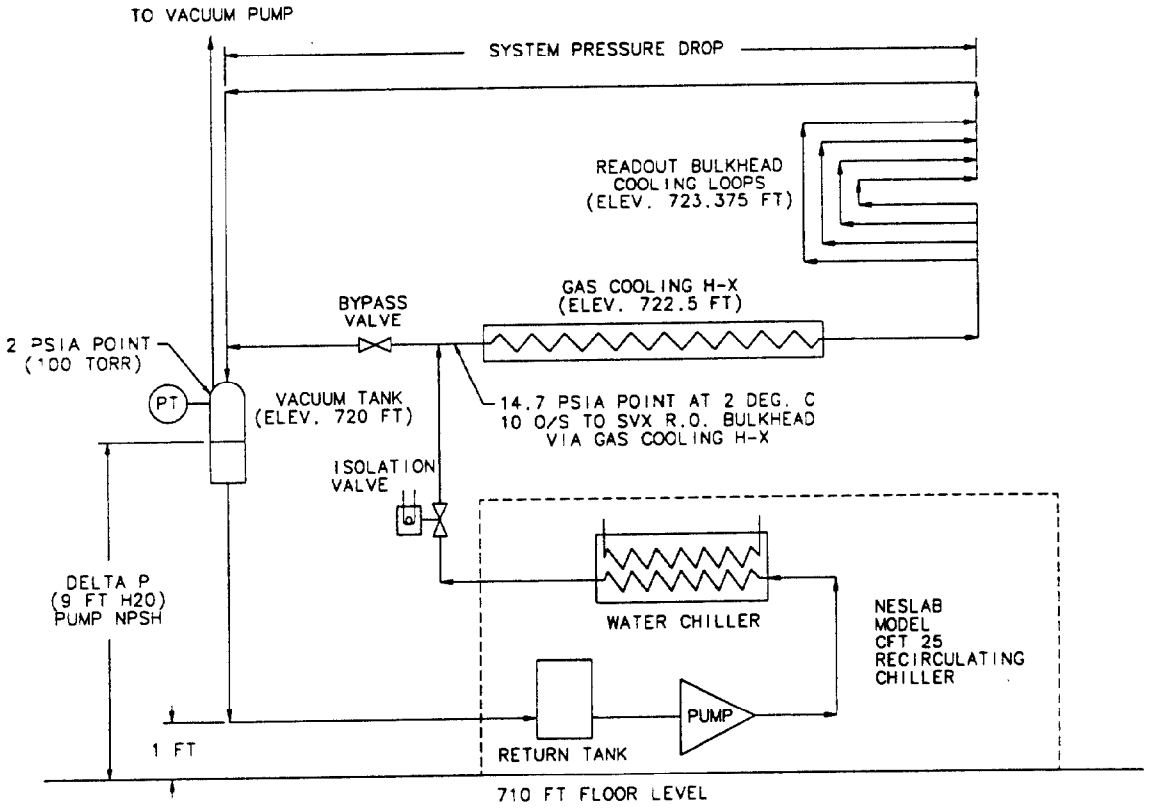


Figure 22

Figure 23



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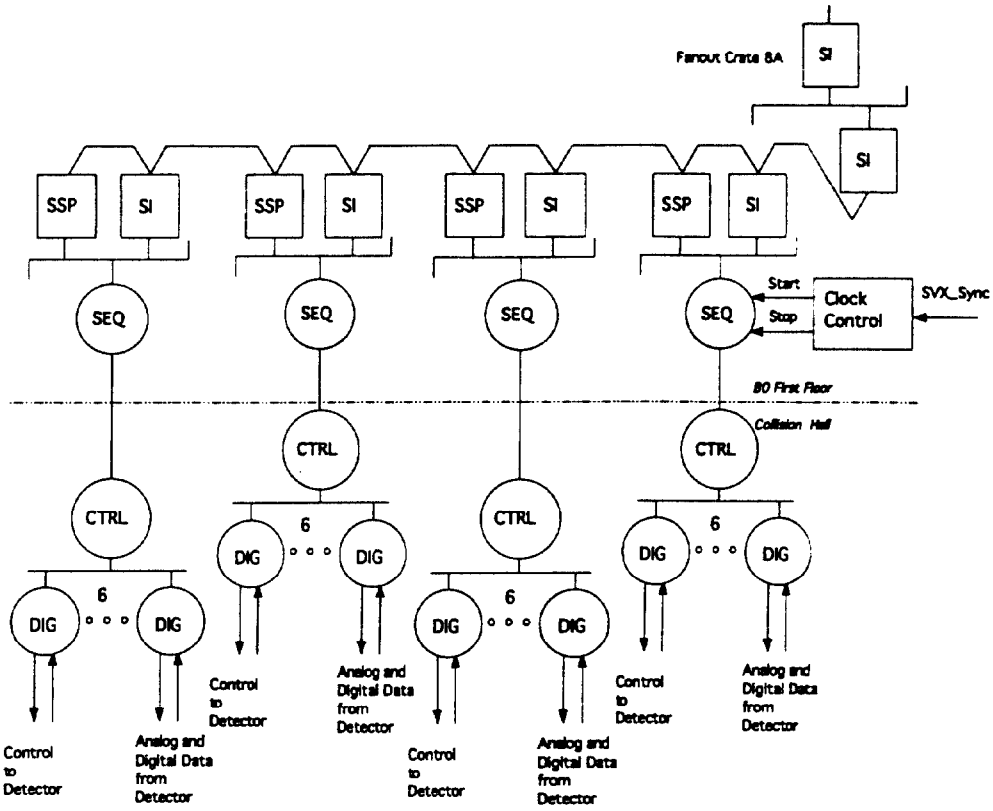
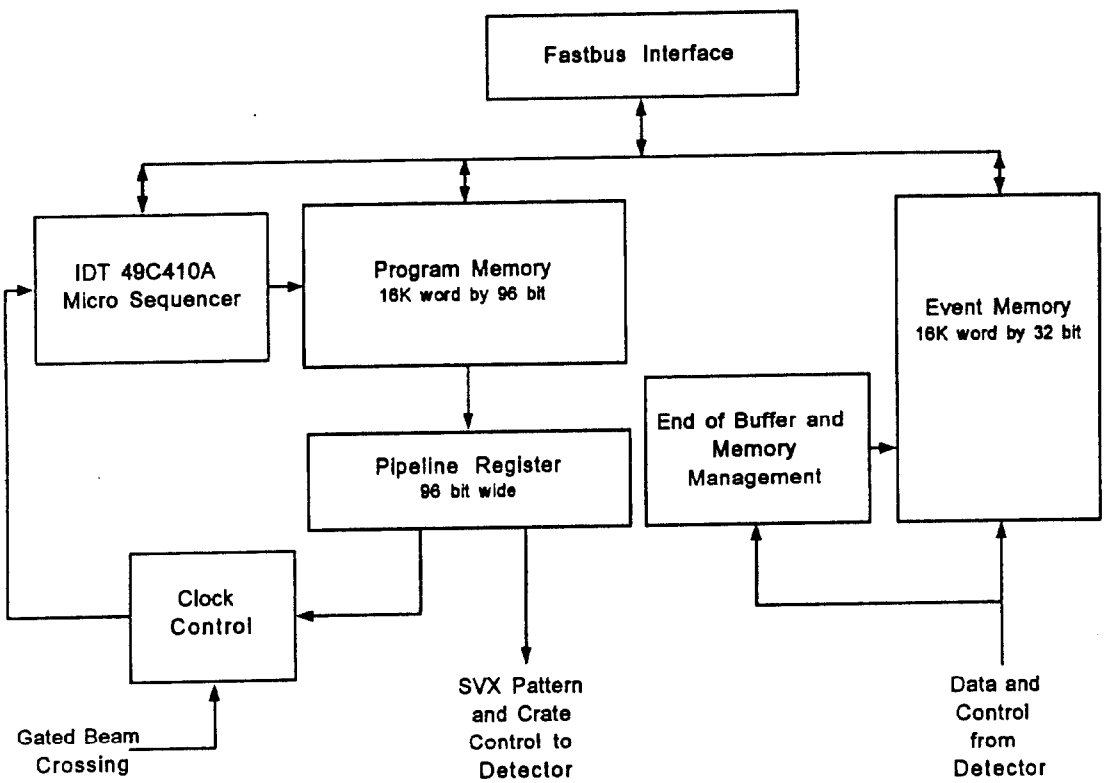


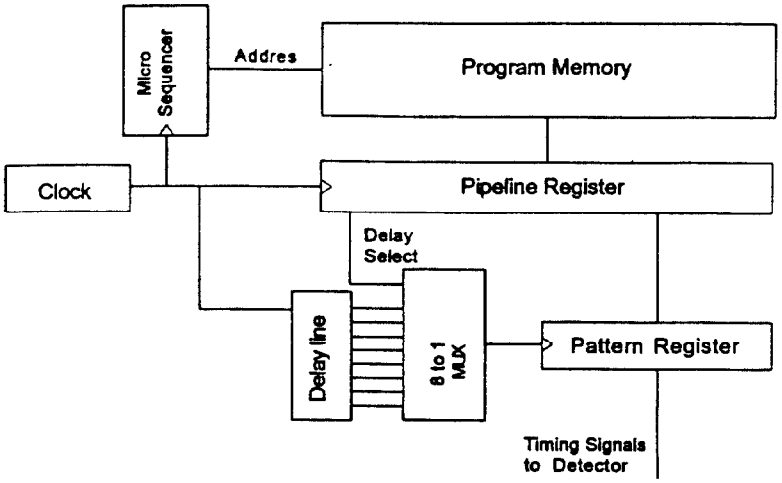
SVX DAQ System Diagram.

Figure 25

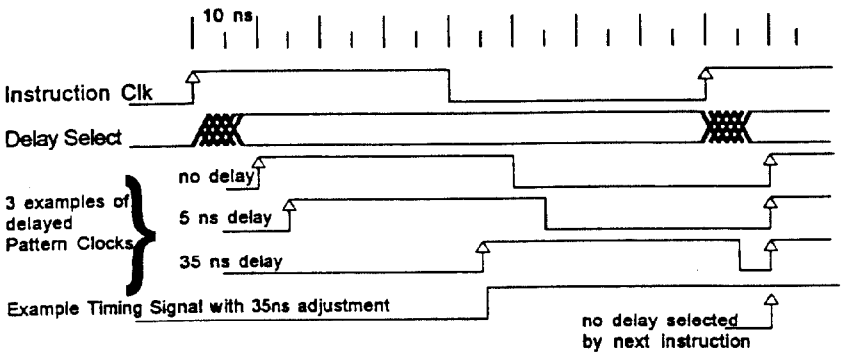


Sequencer Block Diagram.

Figure 26

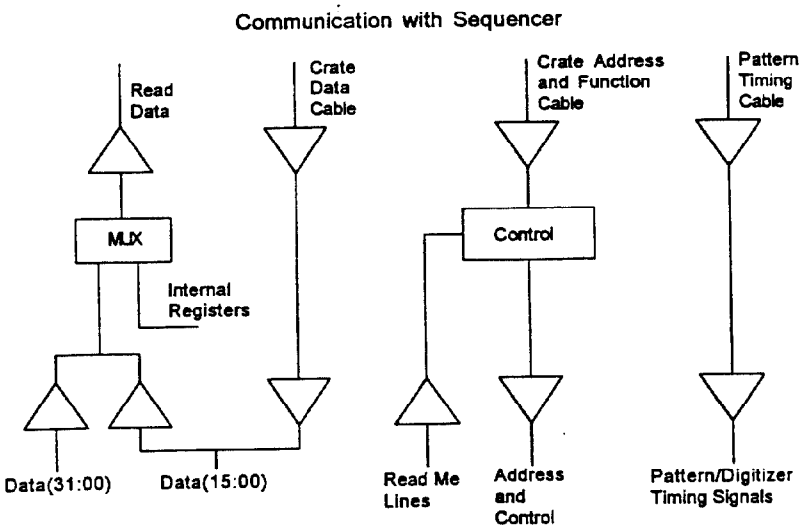


Delayed Clock Timing.



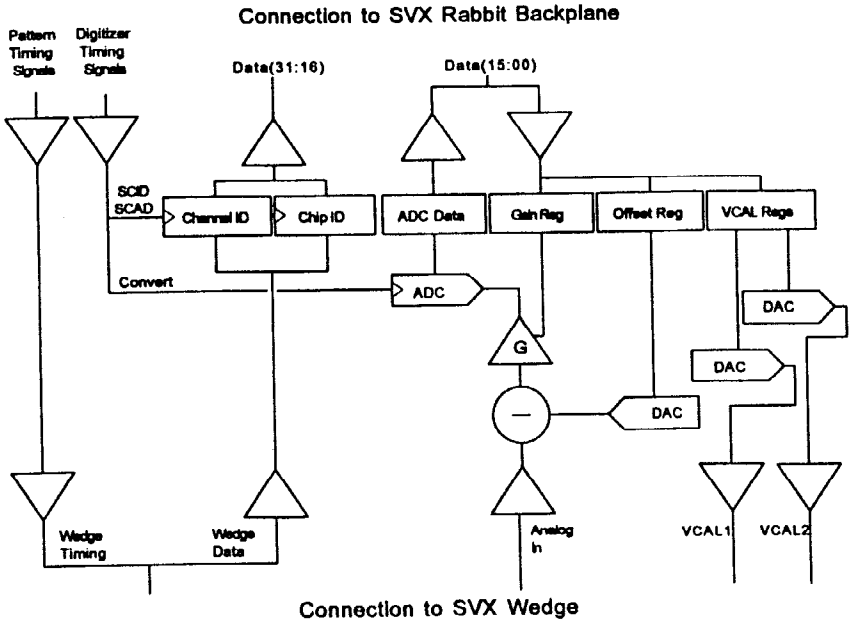
Pattern Timing Block Diagram.

Figure 27



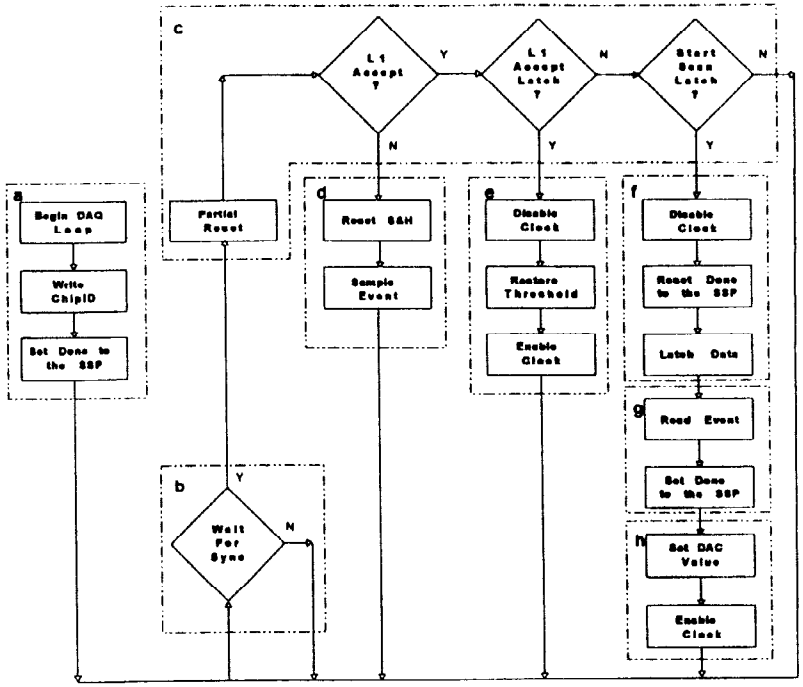
Controller Block Diagram

Figure 28



Digitizer Block Diagram.

Figure 29



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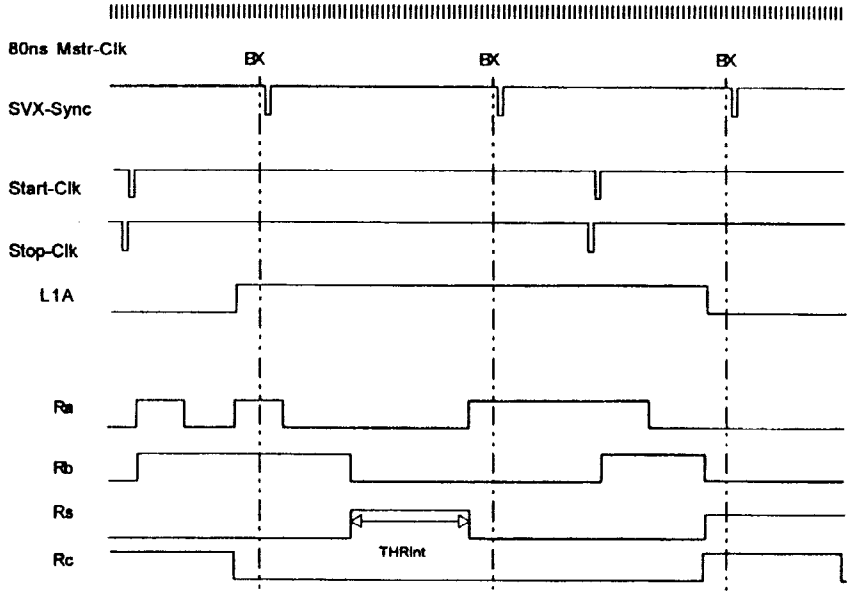

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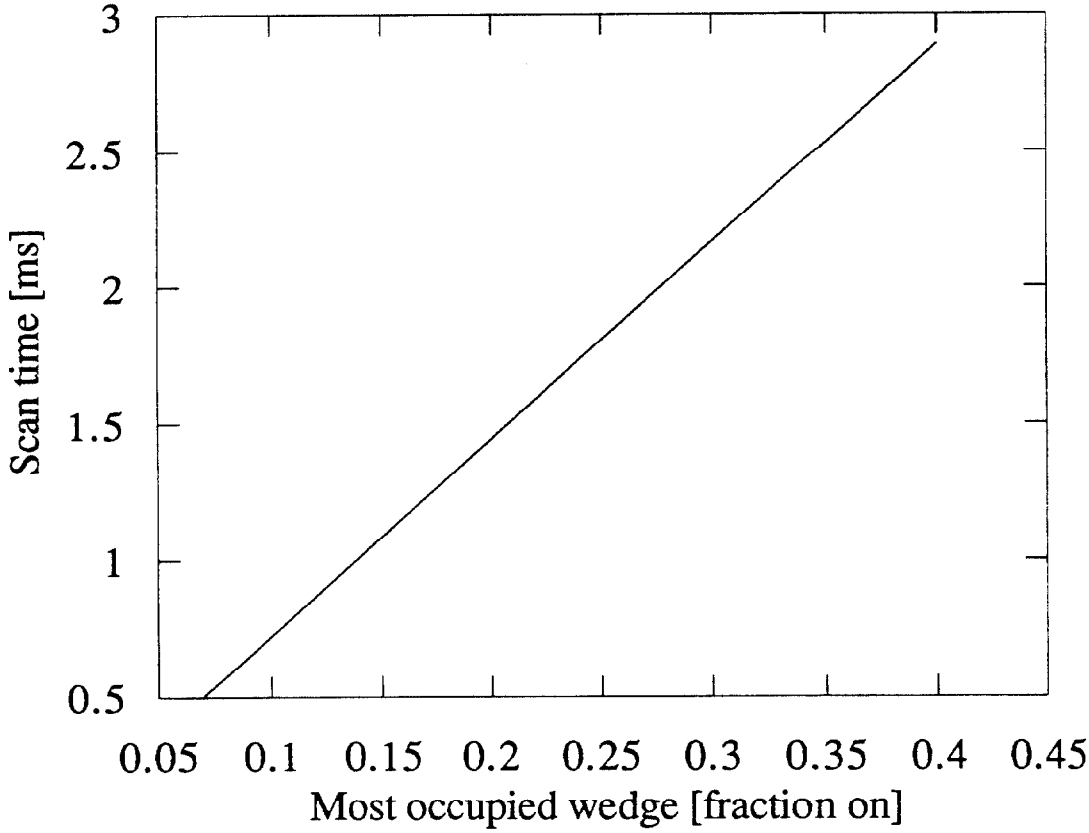

3
2.5
2
1.5
1
0.5
Scan time [ms]
0.05
0.1
0.15
0.2
0.25
0.3
0.35
0.4
0.45
Most occupied wedge [fraction on]

Figure 32

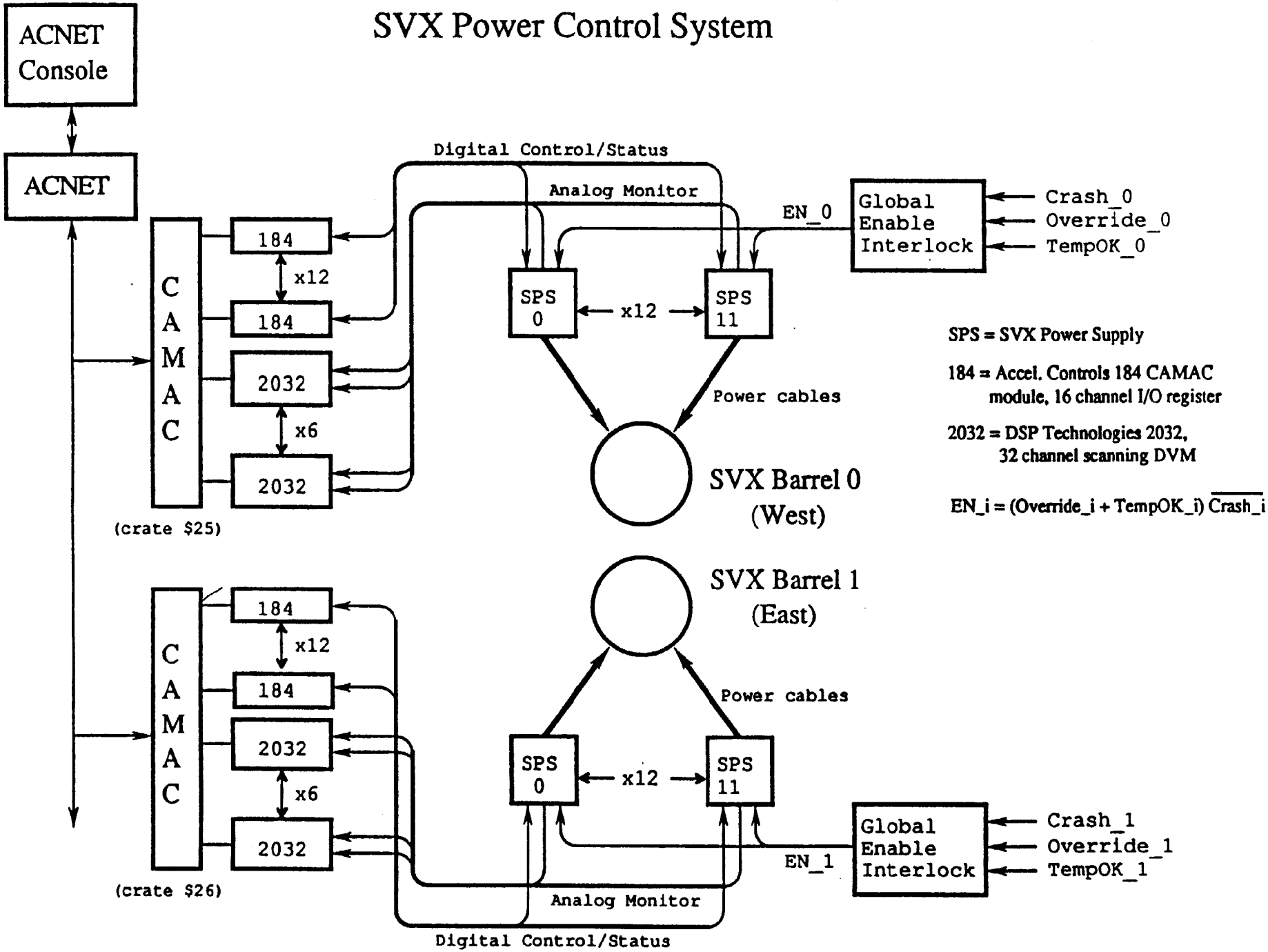
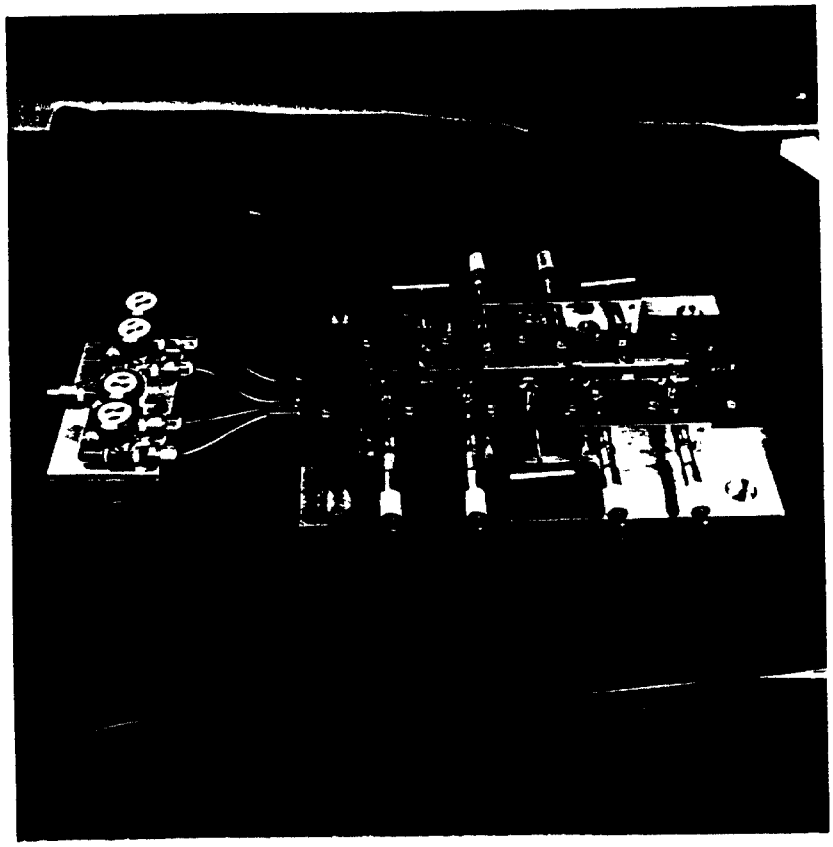


Figure 33

Block diagram indicating elements of the power supply, control, and monitoring system for the SVX.



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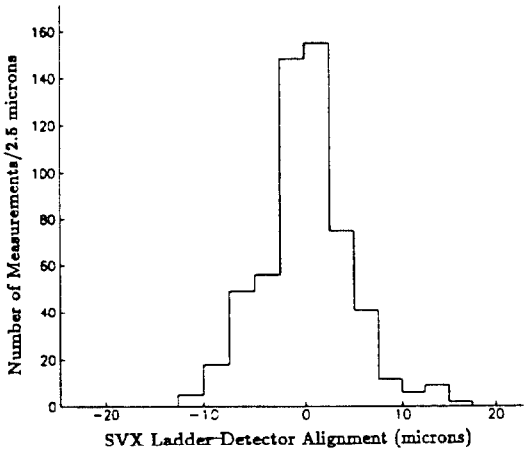

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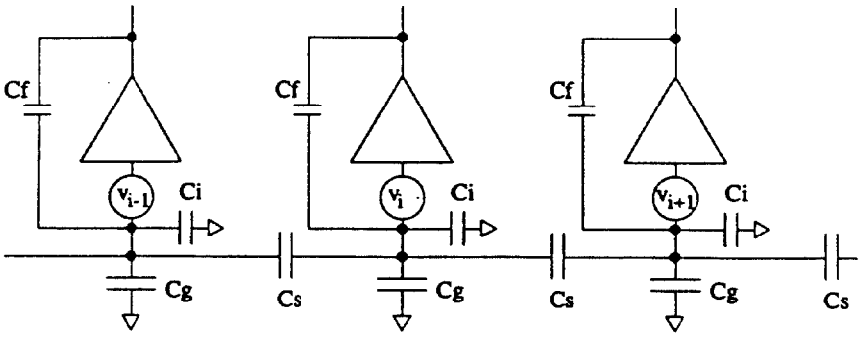

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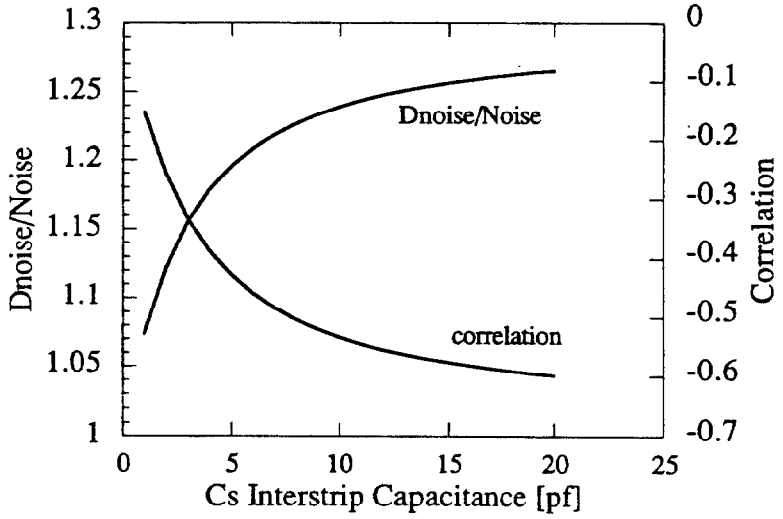

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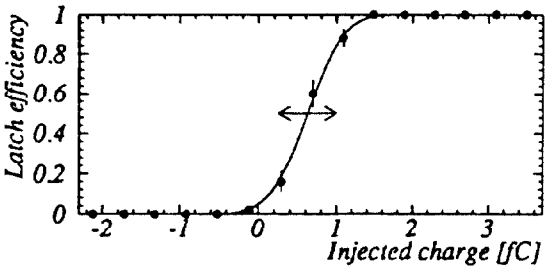

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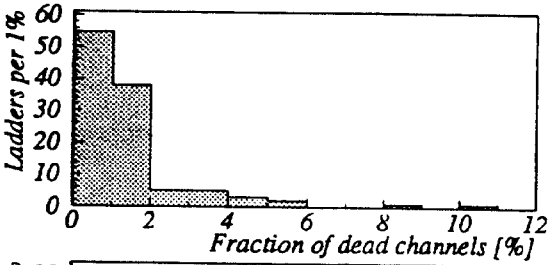
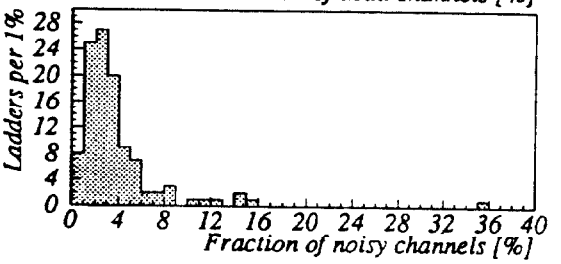


Figure 39



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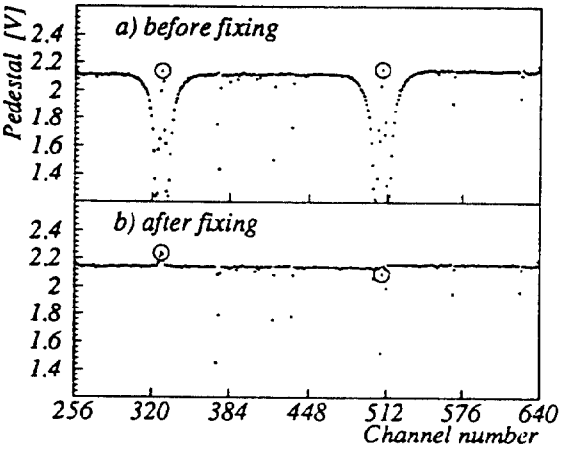


Figure 41a,b

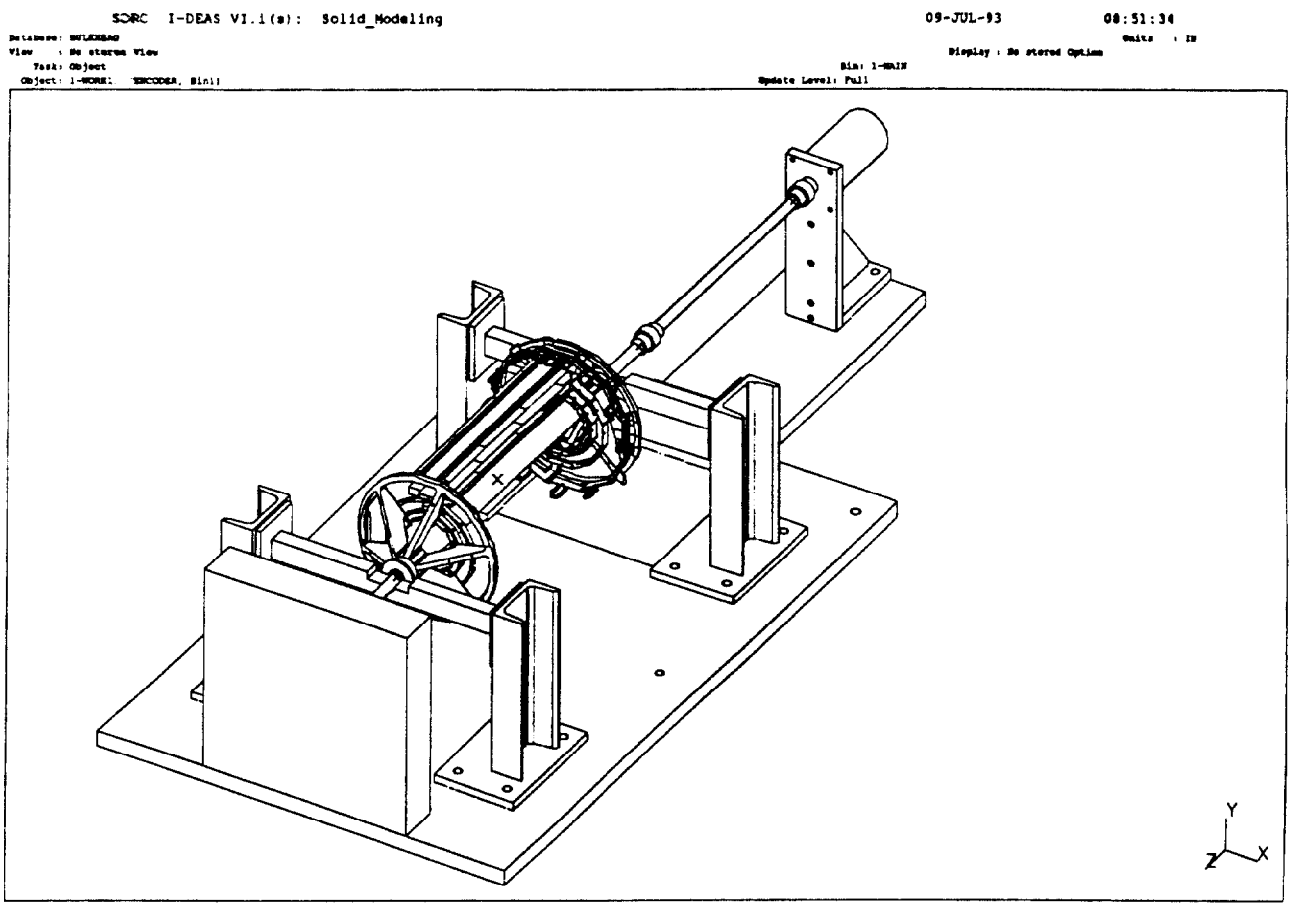


Figure 42

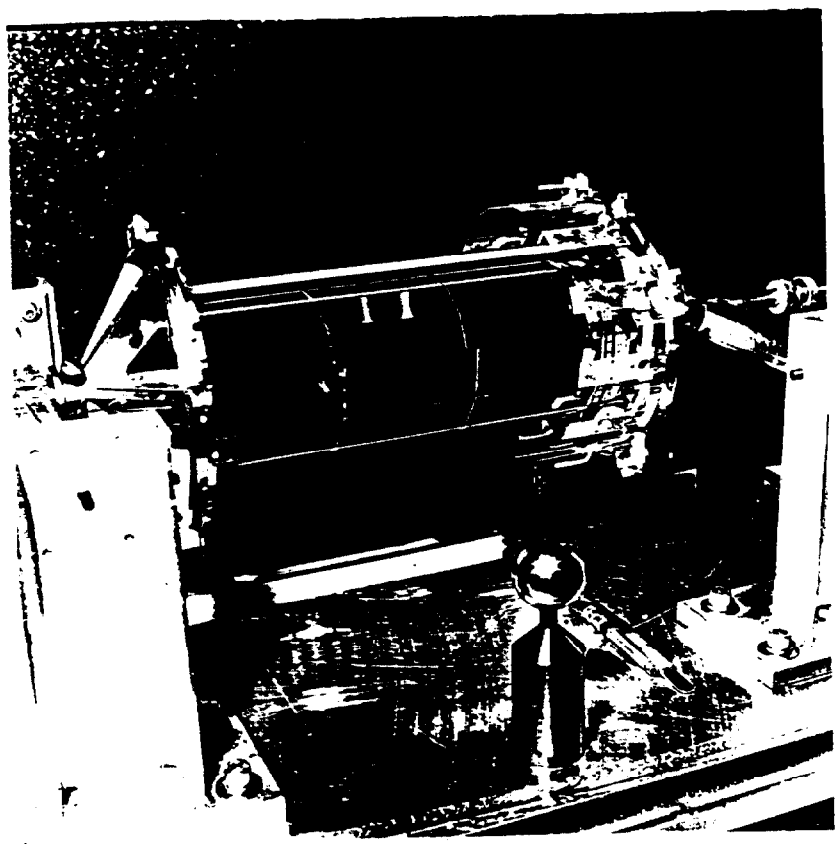
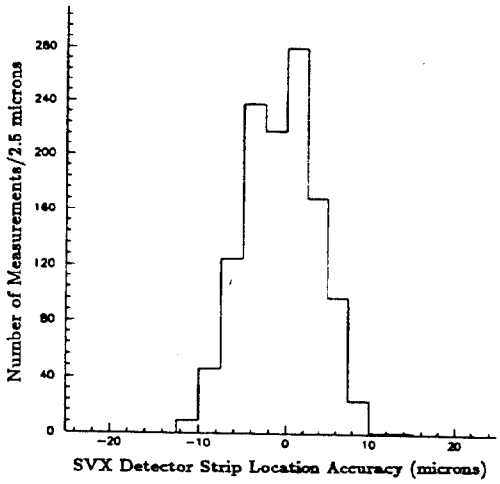


Figure 43



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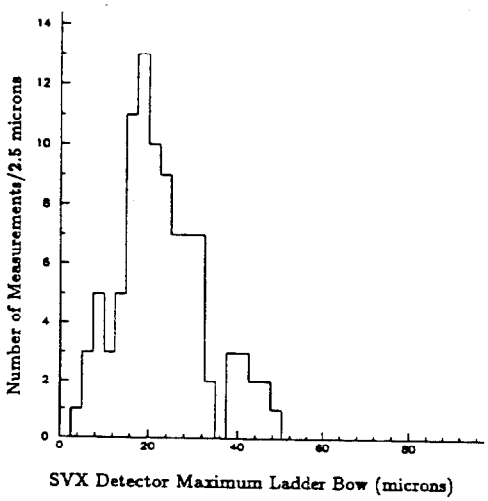

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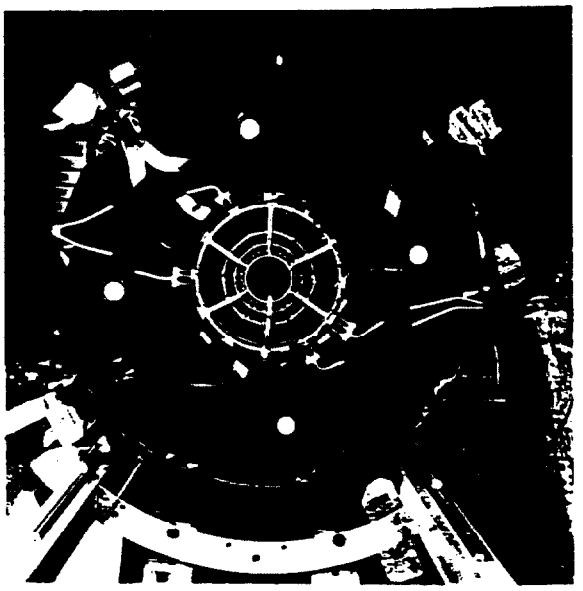

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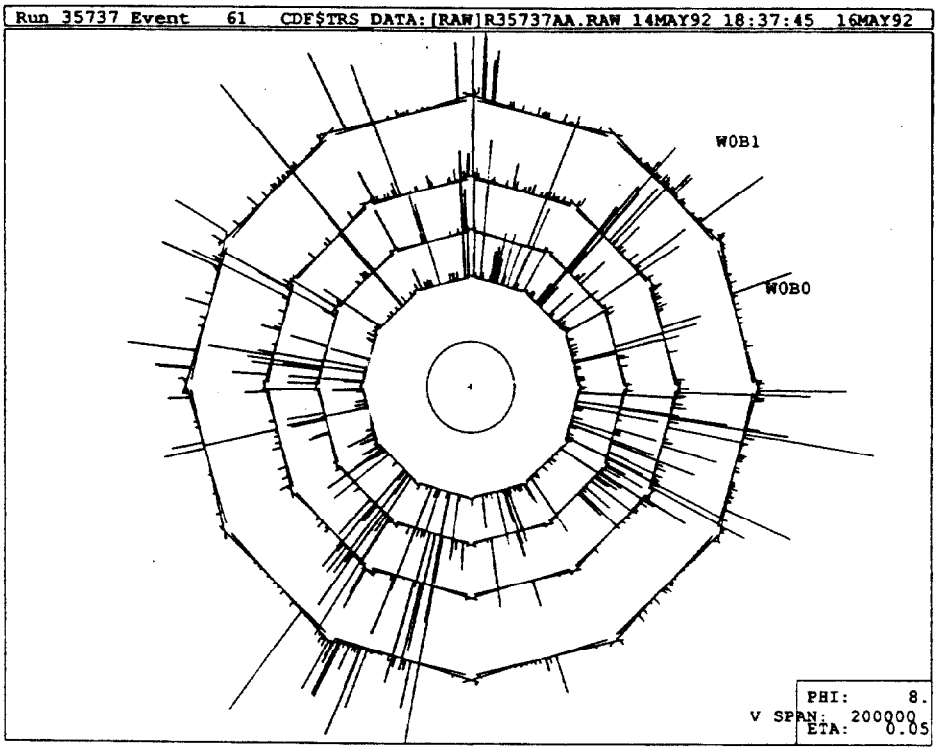


Figure 47

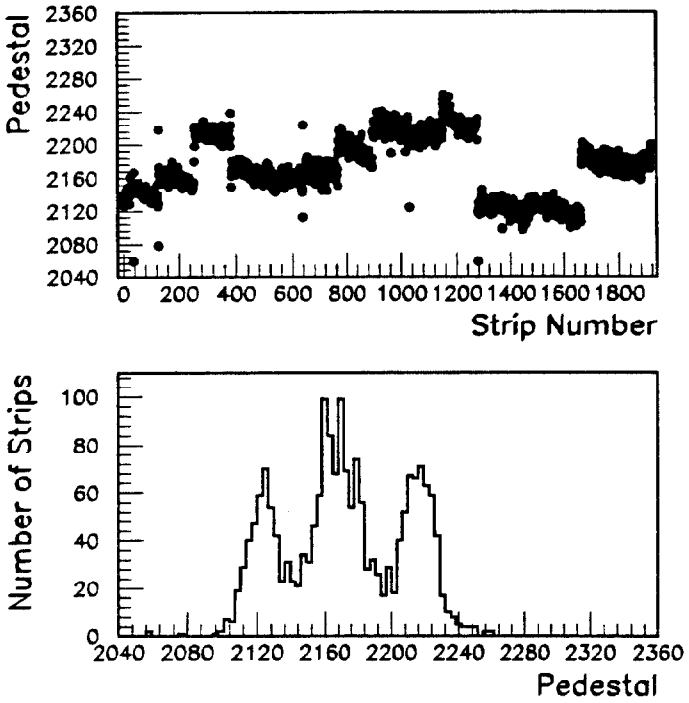


Figure 48a,b

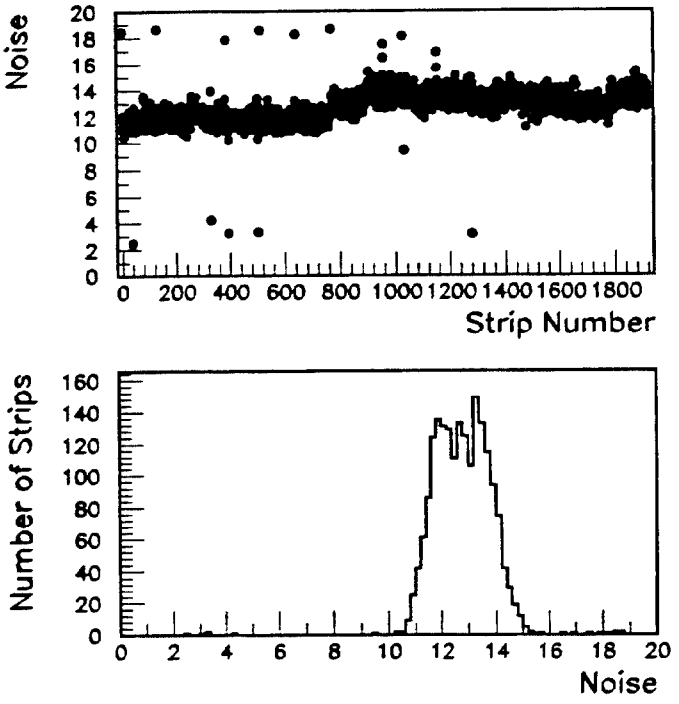


Figure 49a,b

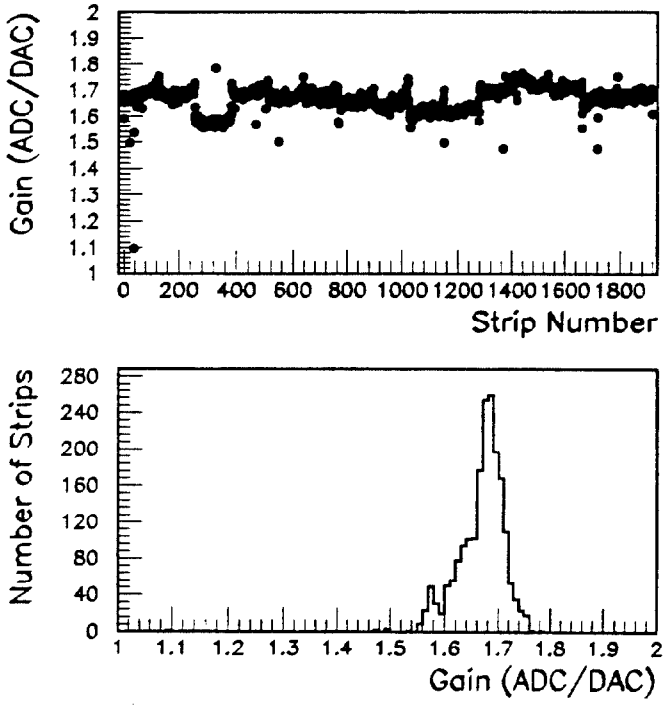


Figure 50a,b

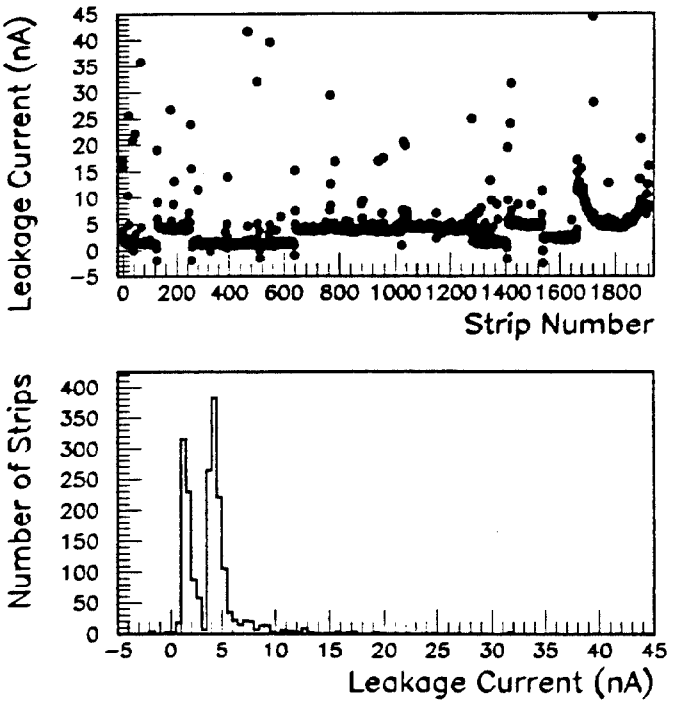


Figure 51a,b

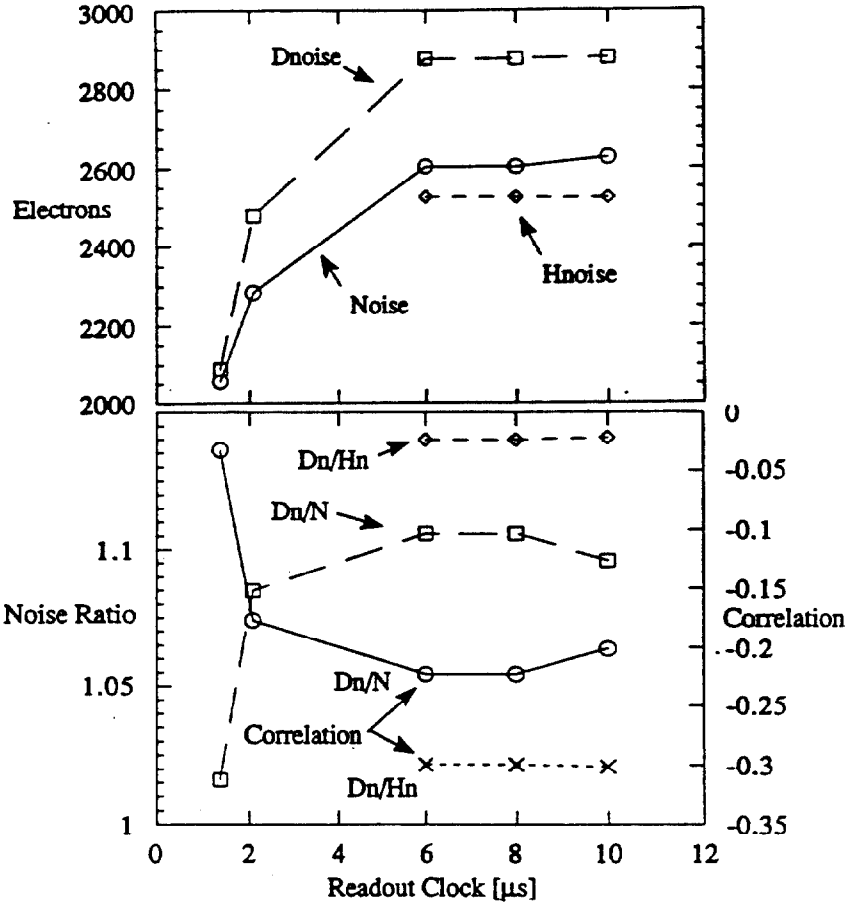


Figure 52

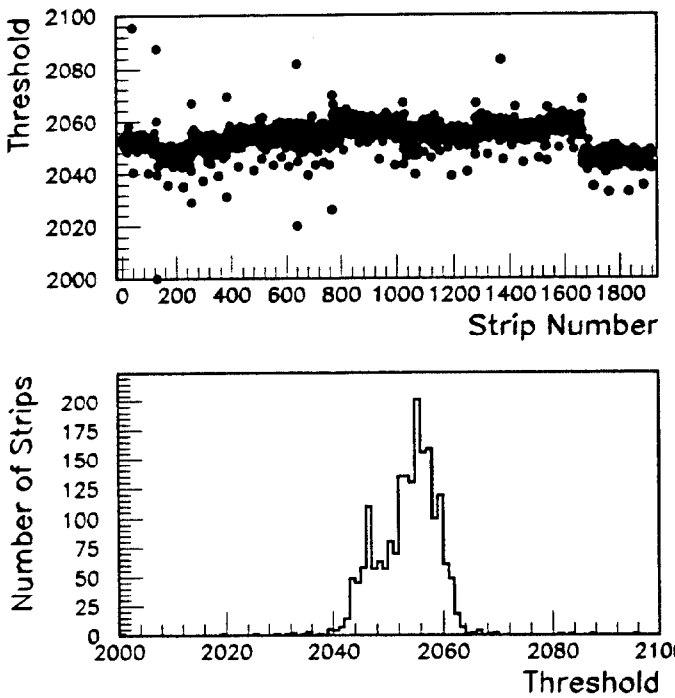


Figure 53a,b

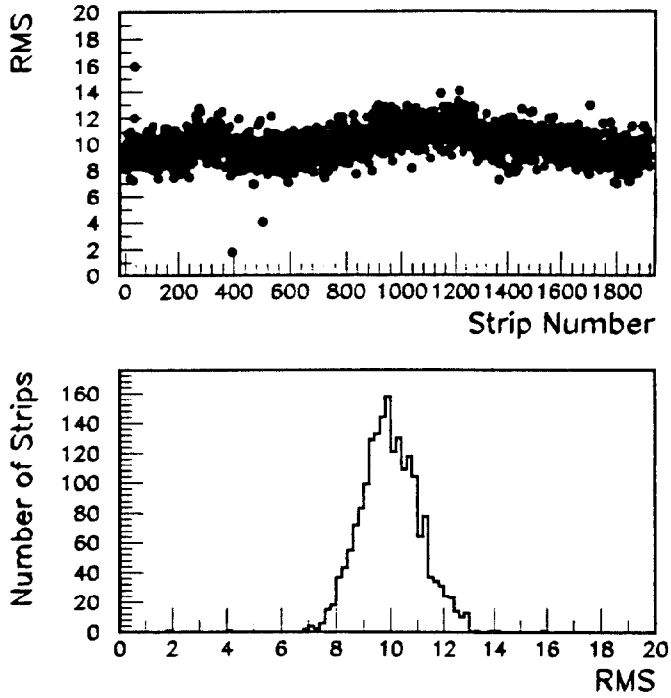


Figure 53c,d

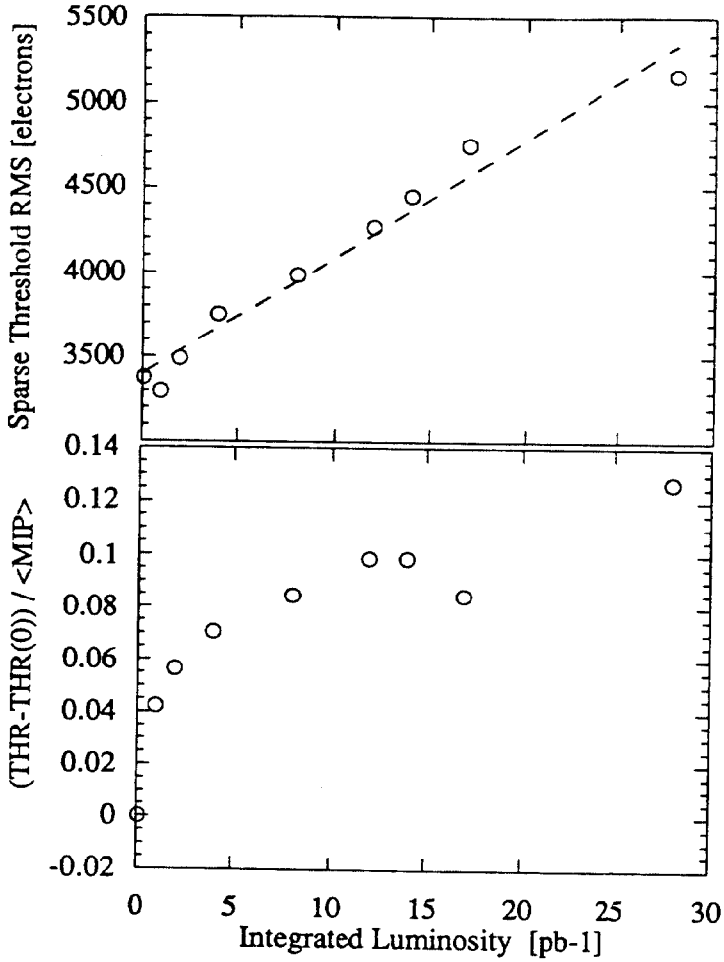


Figure 54a,b

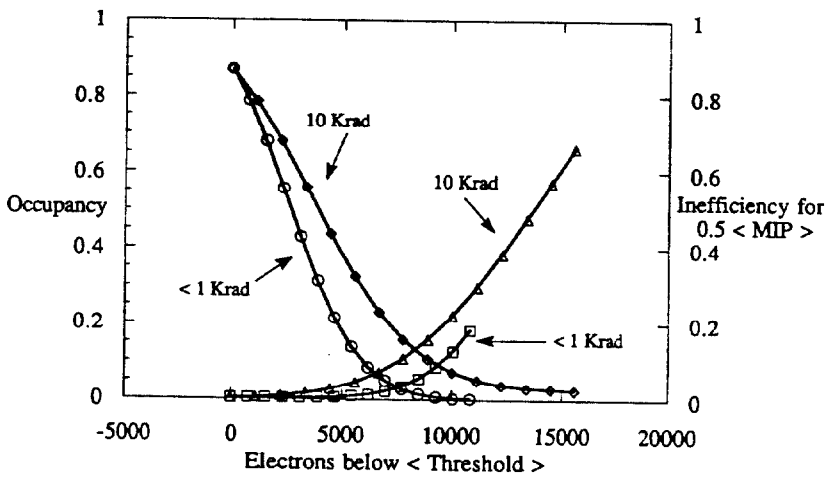


Figure 55

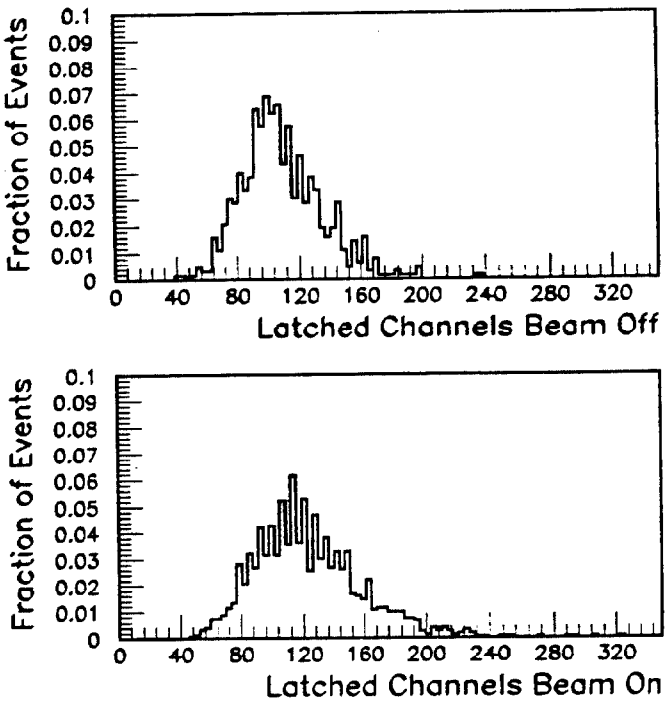


Figure 56a,b

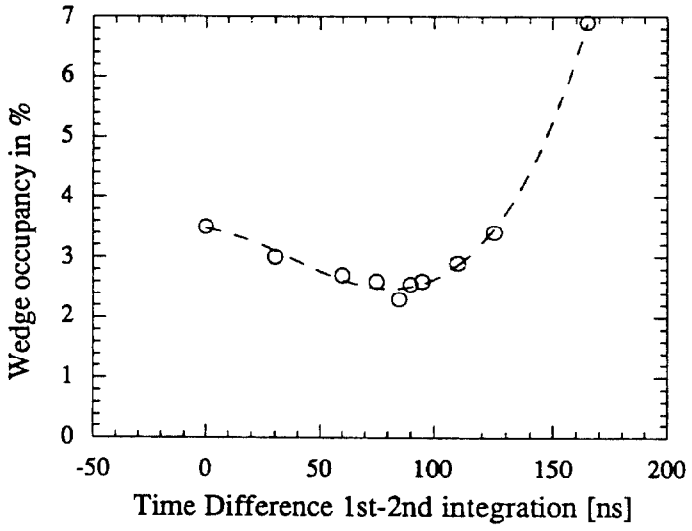


Figure 57

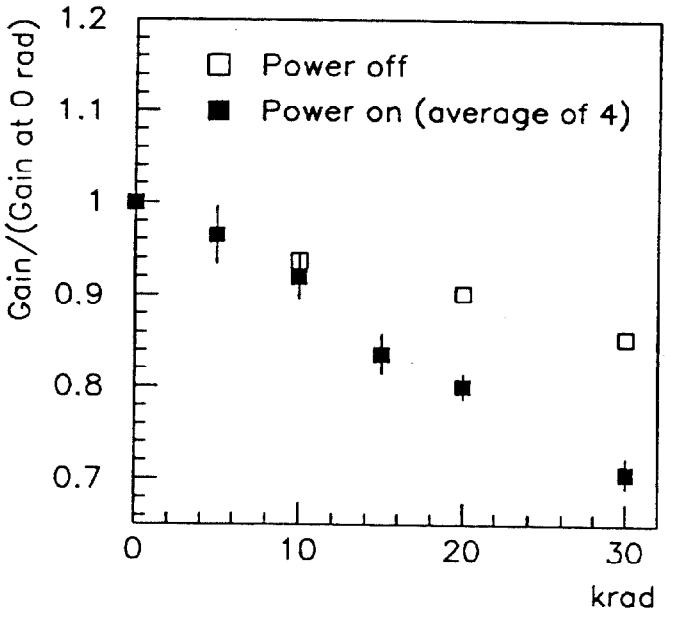


Figure 58

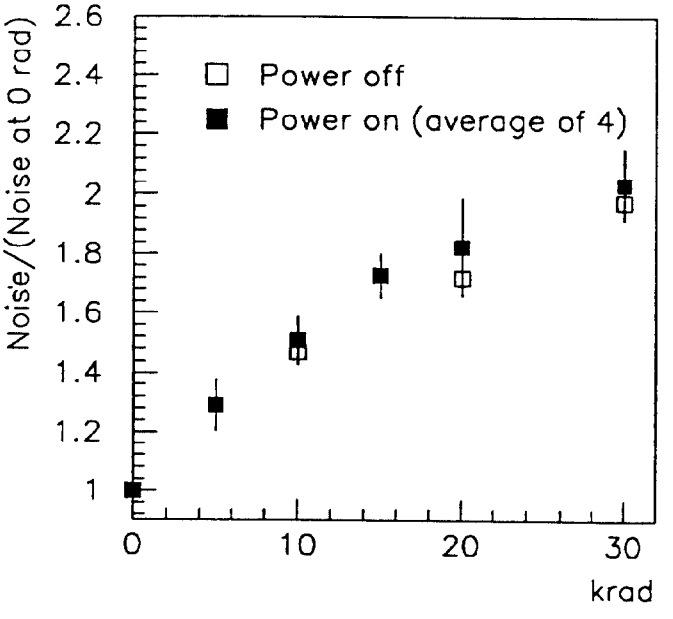


Figure 59

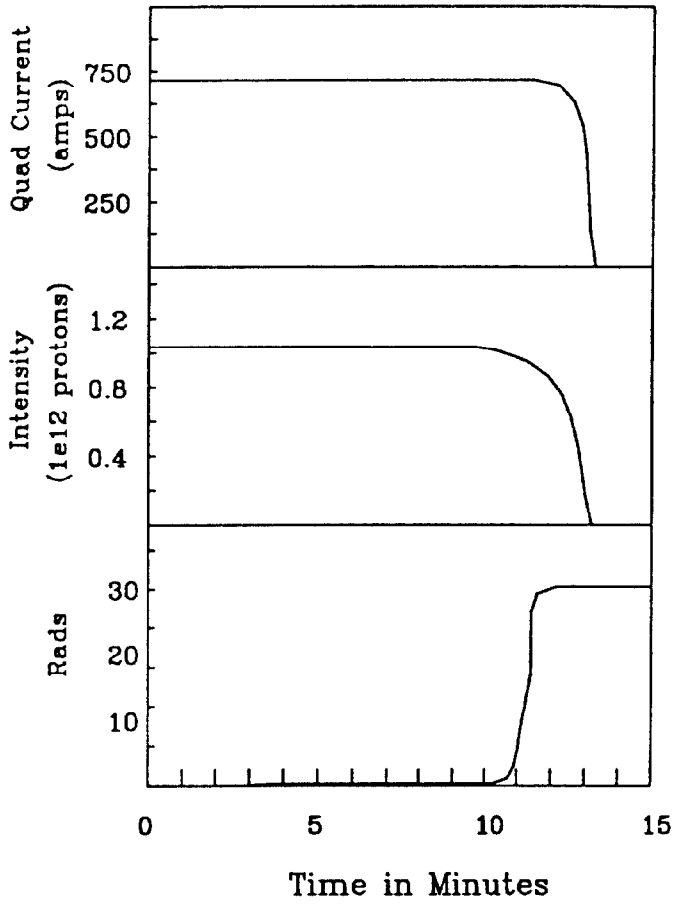


Figure 60a,b,c

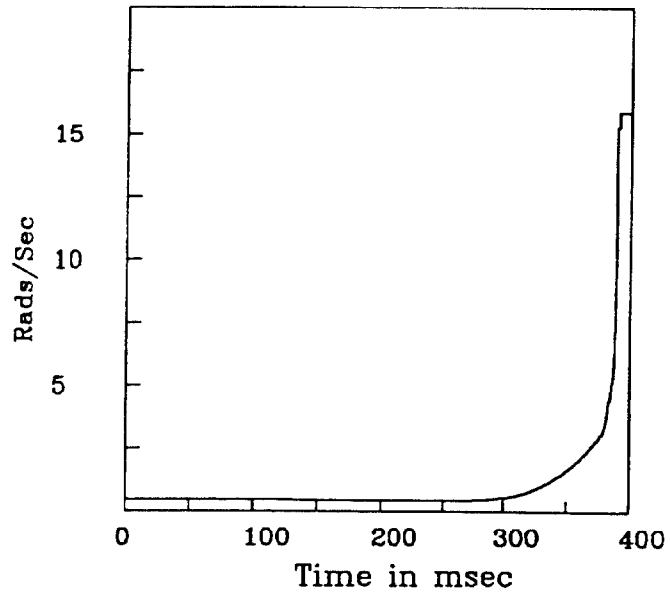


Figure 60d

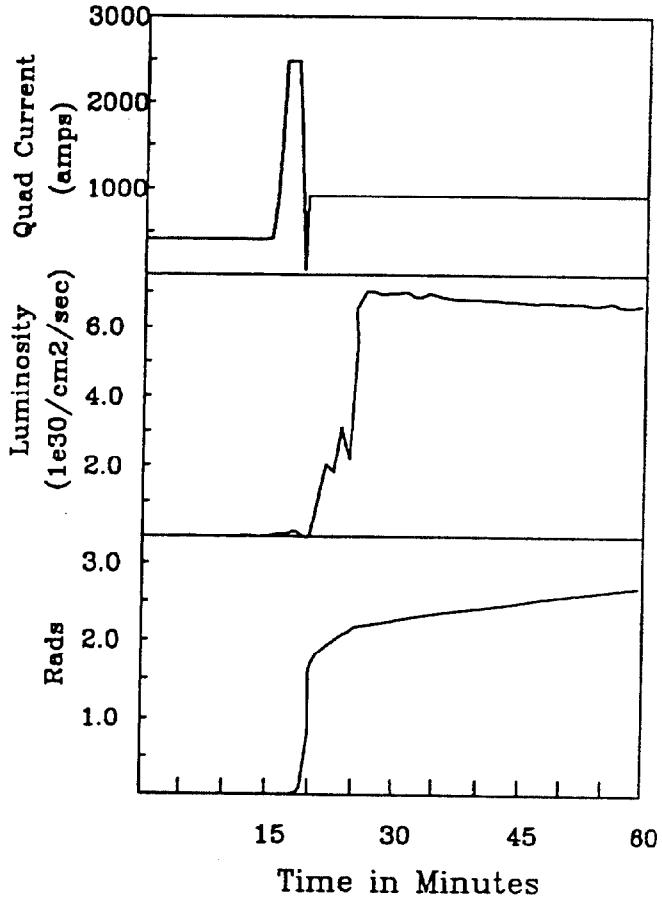

3000
2000
1000
Quad Current
(amps)
Luminosity
(1e30/cm2/sec)
6.0
4.0
2.0
3.0
2.0
1.0
Rads
15
30
45
60
Time in Minutes

Figure 61

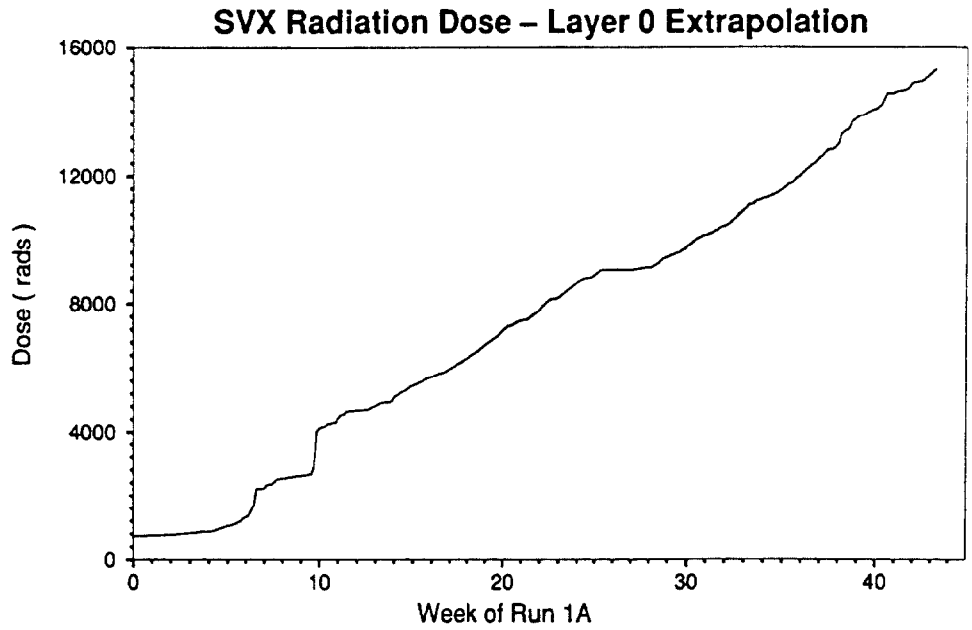


Figure 62

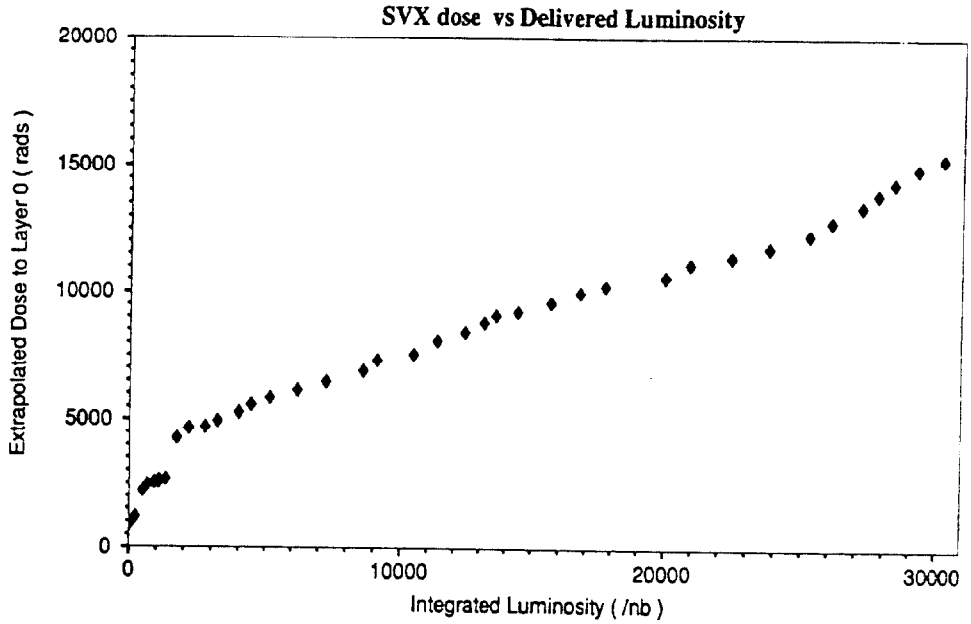


Figure 63

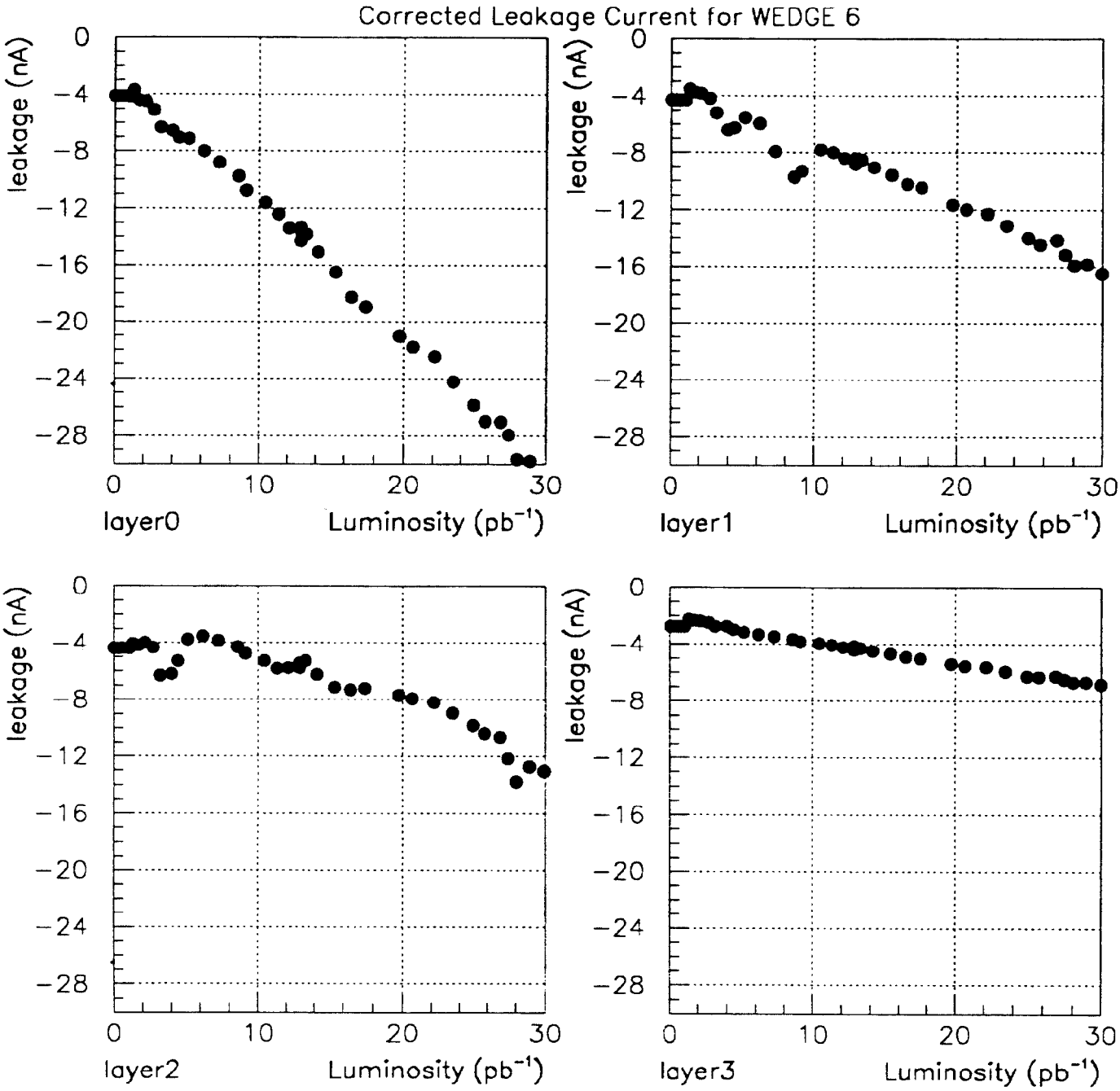


Figure 64a,b,c,d

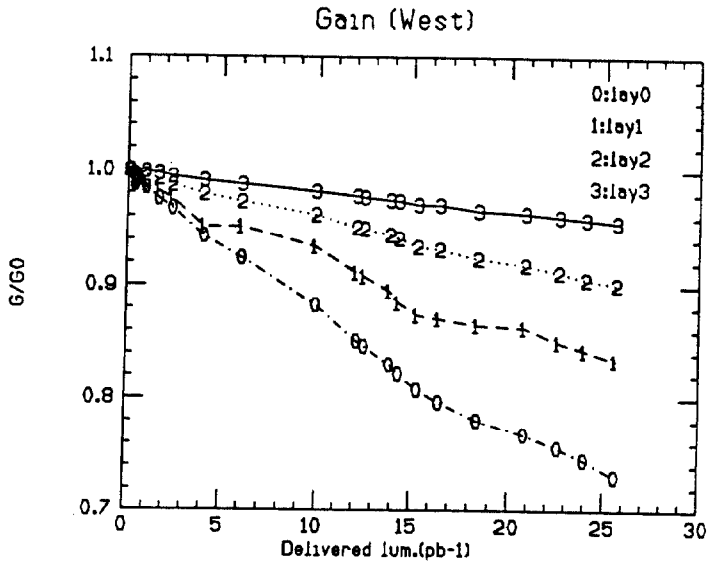


Figure 65

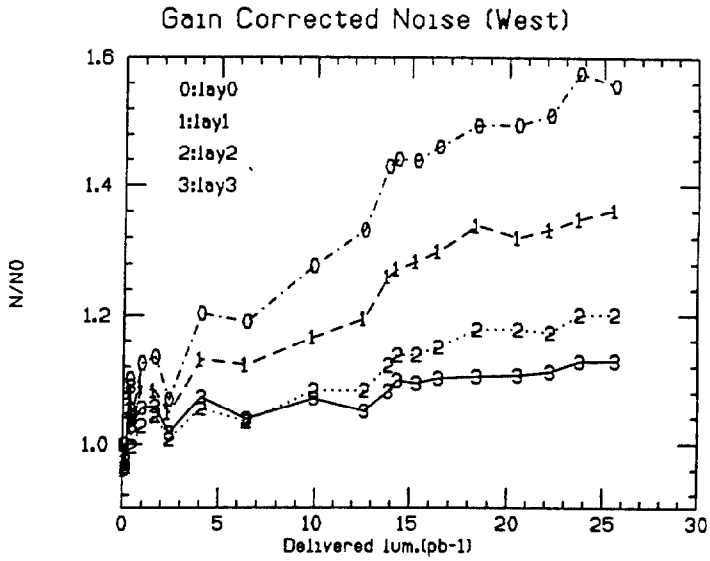


Figure 66

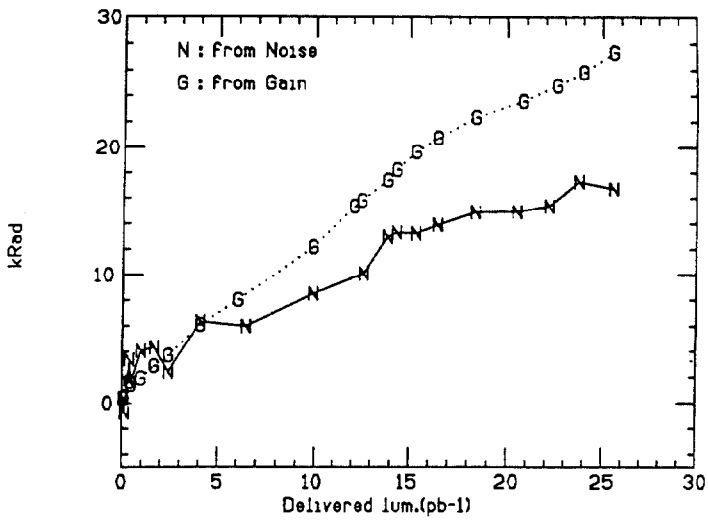


Figure 67

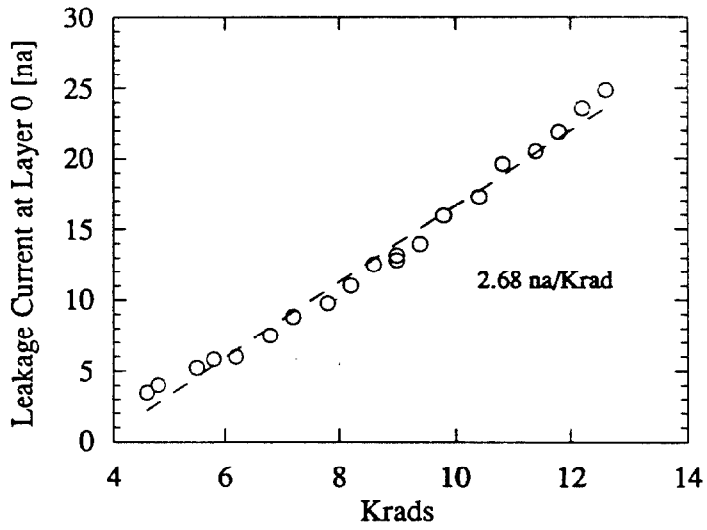


Figure 68

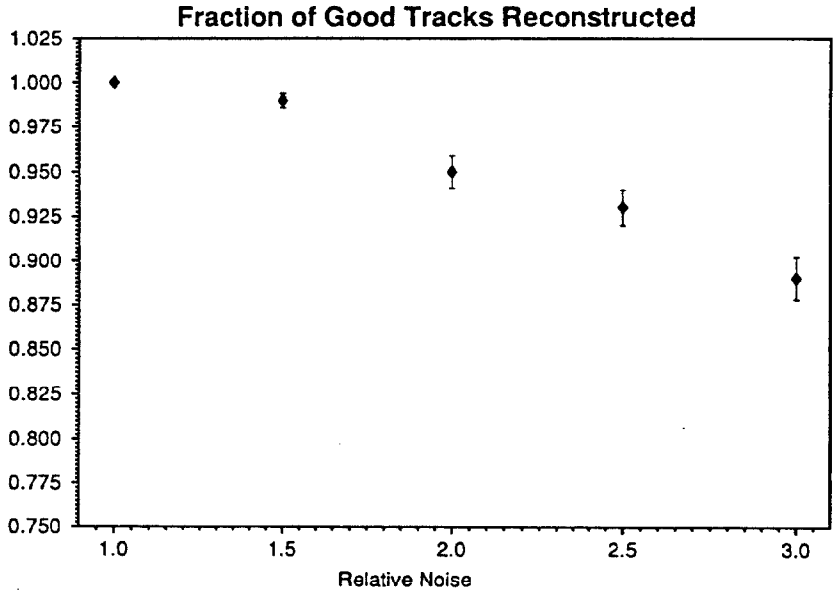


Figure 69

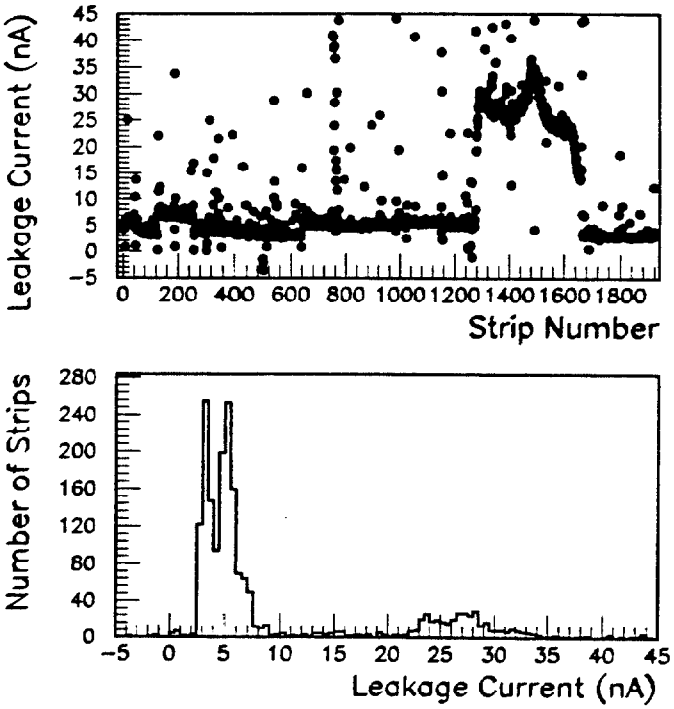


Figure 70a,b

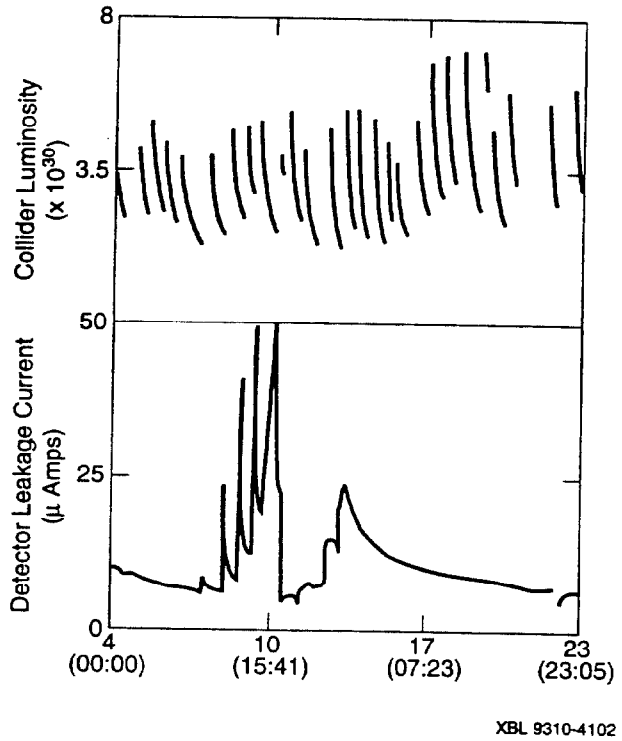


Figure 71

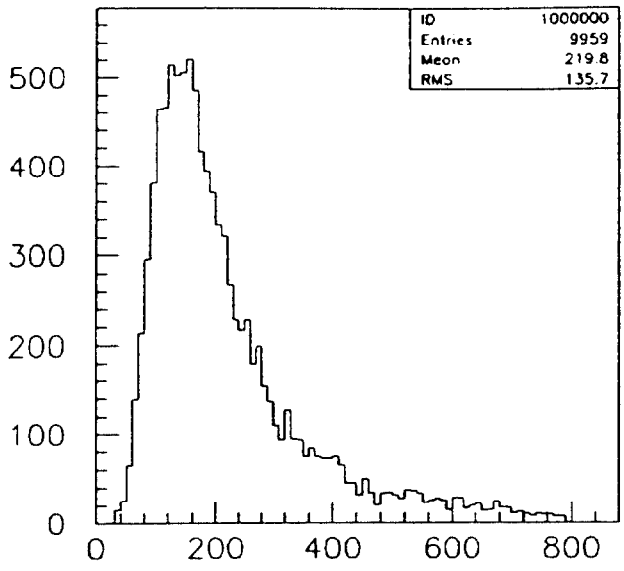


Figure 72a

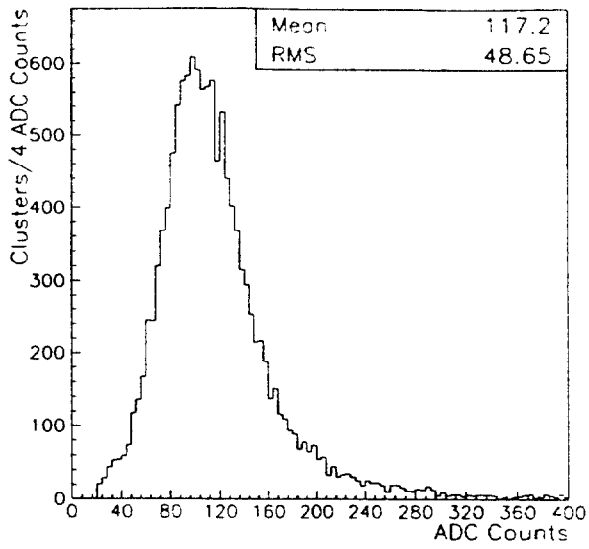


Figure 72b

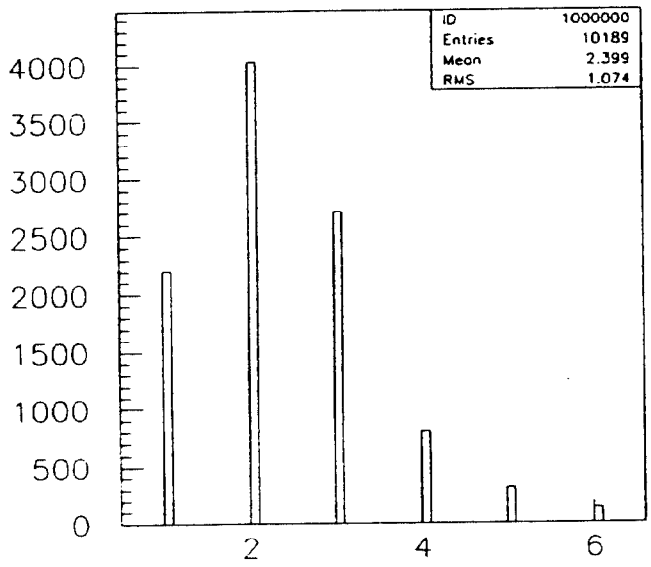


Figure 73

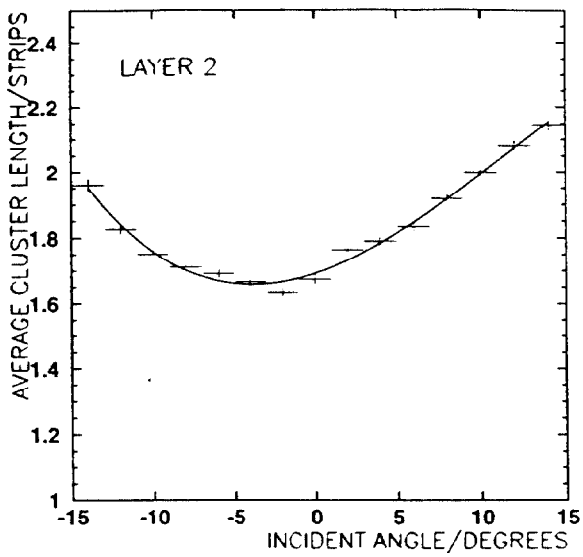


Figure 74

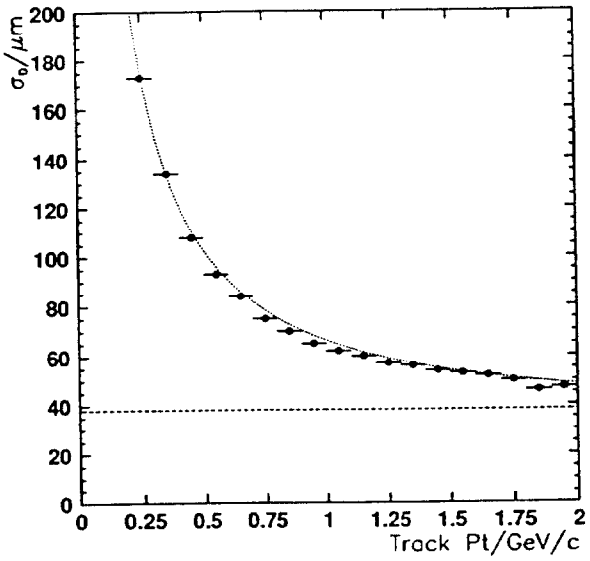


Figure 75

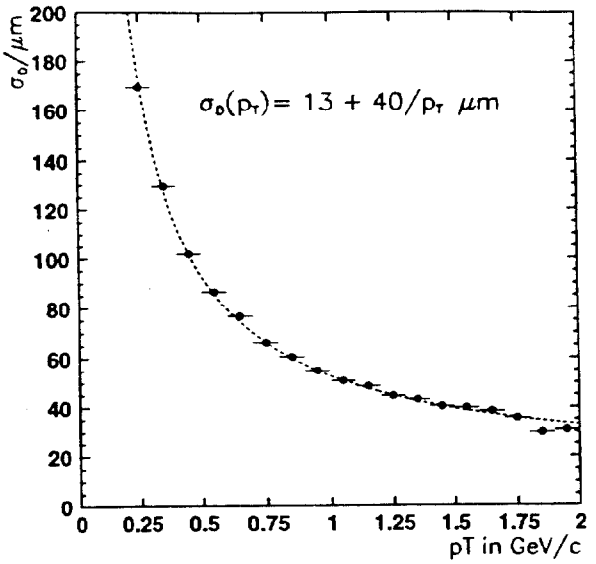


Figure 76

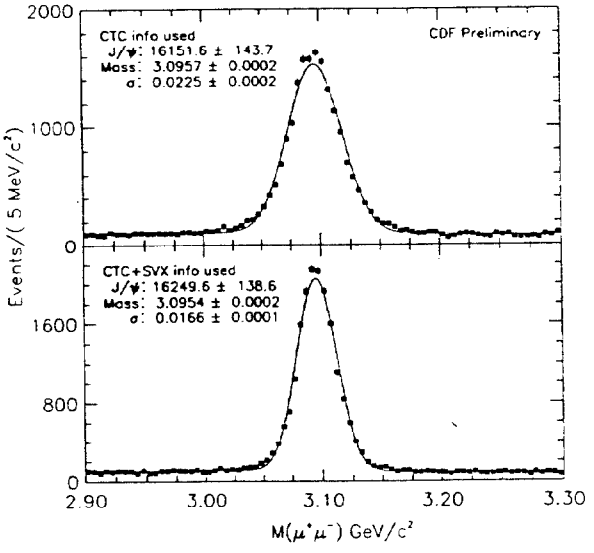


Figure 77

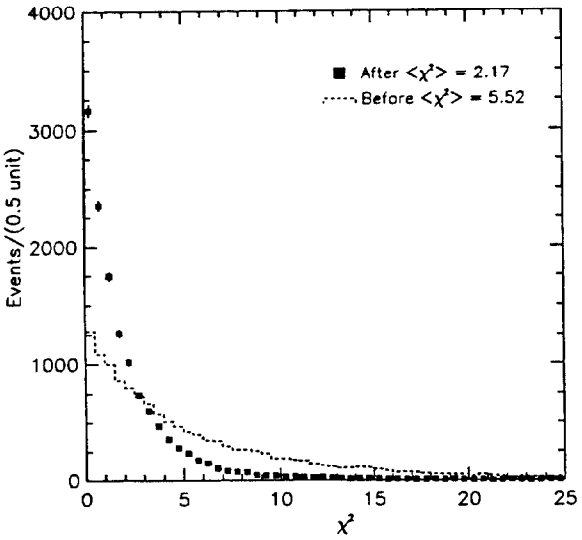


Figure 78

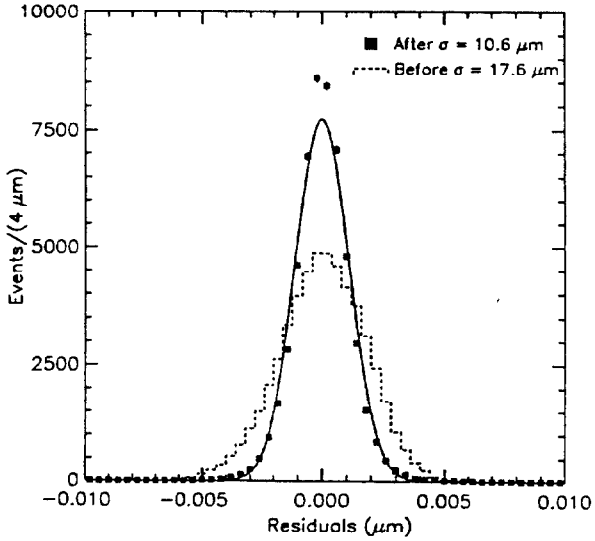


Figure 79

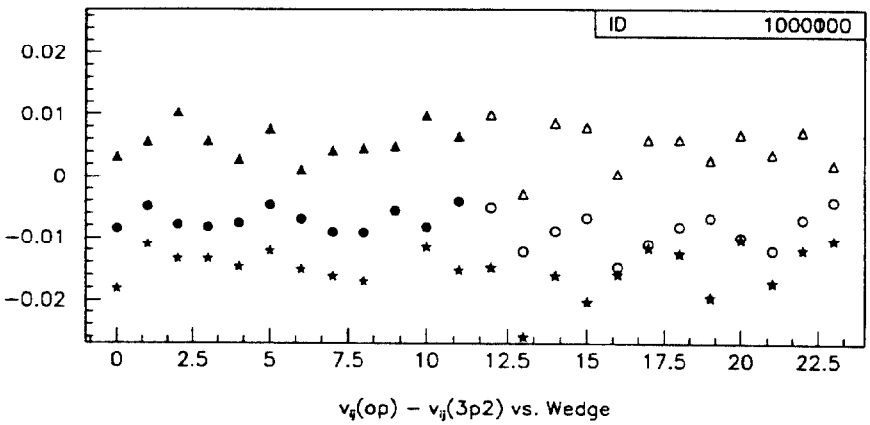


Figure 80

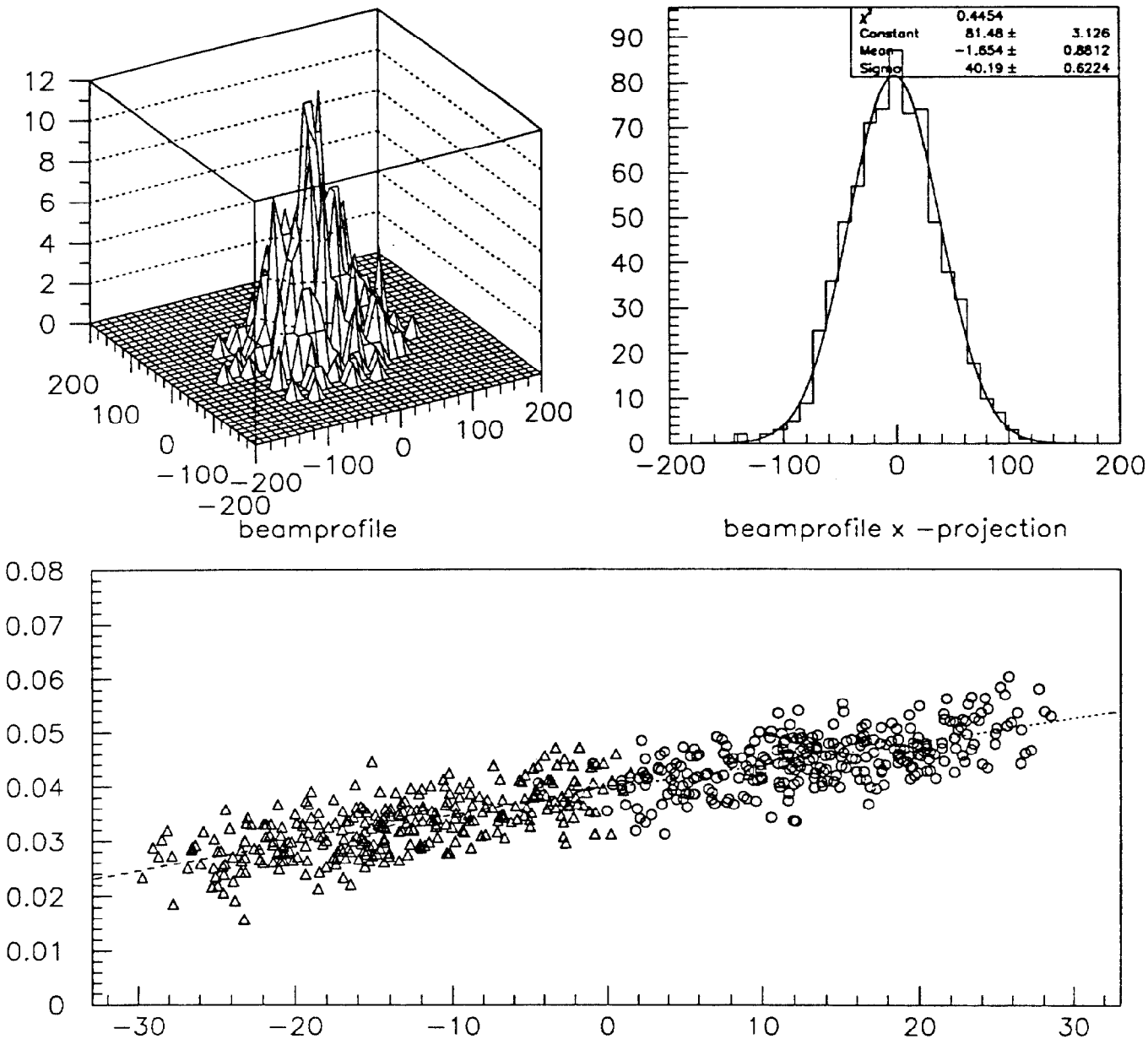

beamprofile
beamprofile x −projection
χ² 0.4454
Constant 81.48 ± 3.126
Mean −1.654 ± 0.8812
Sigma 40.19 ± 0.6224

Figure 81

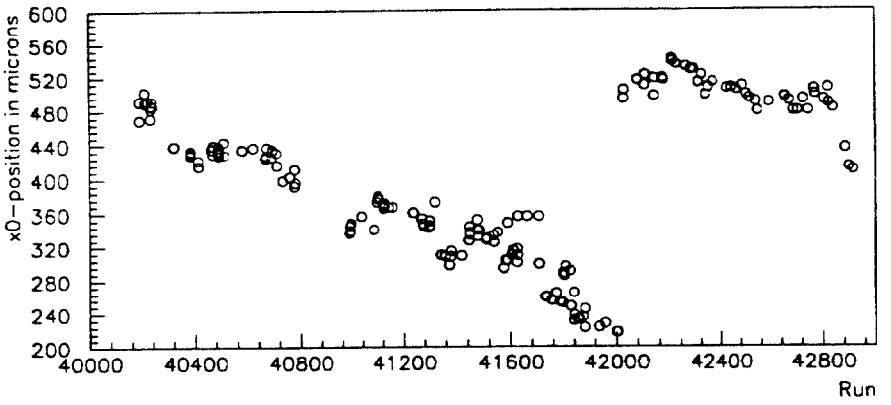


Figure 82a

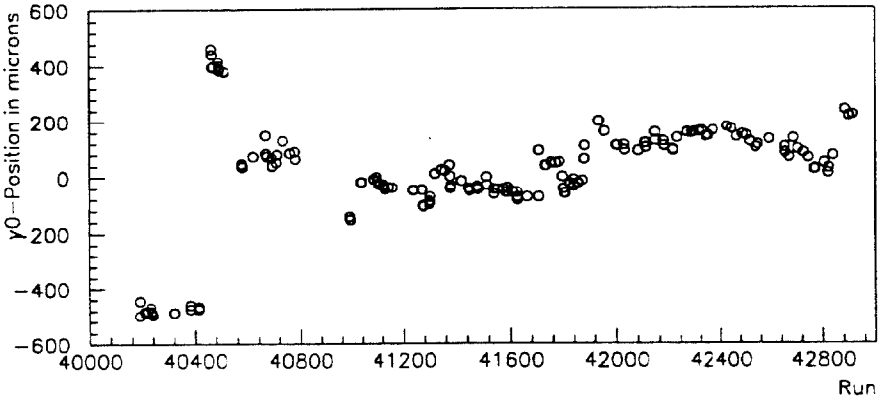


Figure 82b

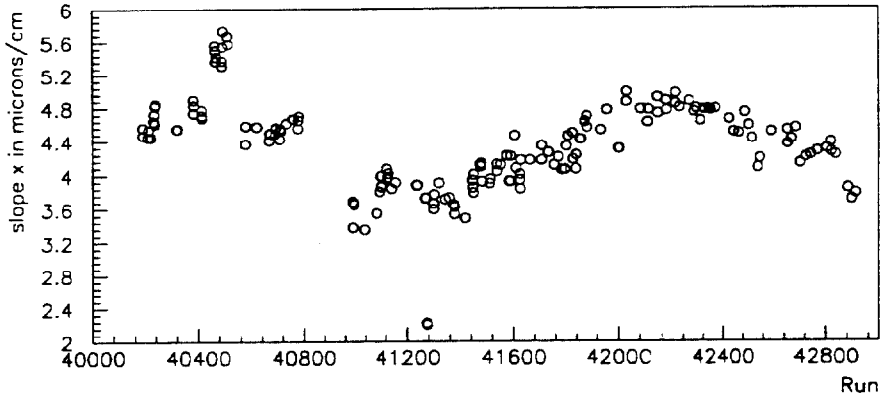


Figure 83a

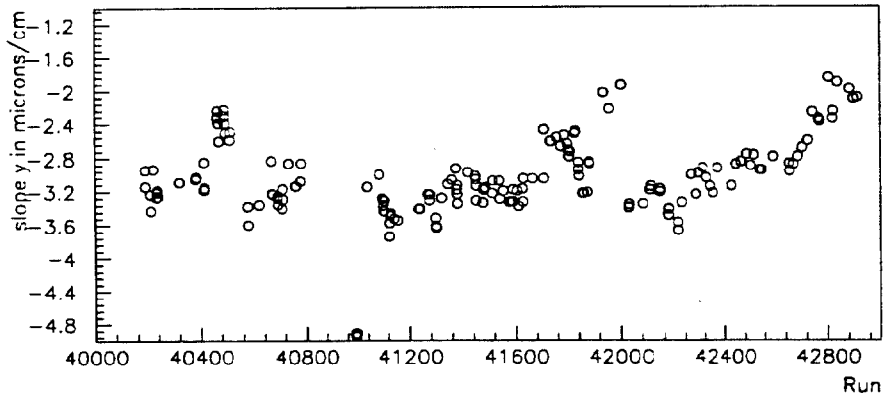


Figure 83b

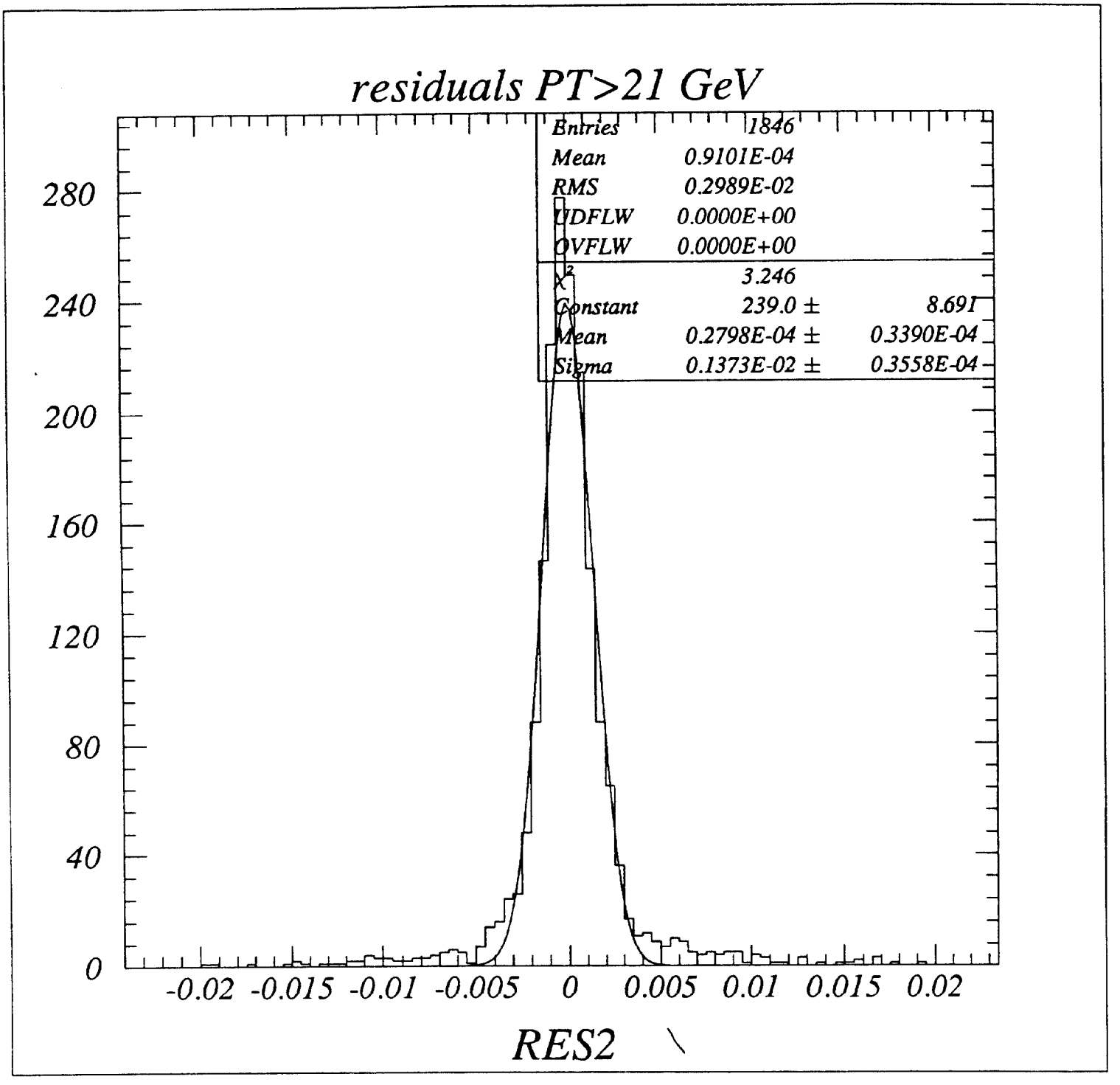
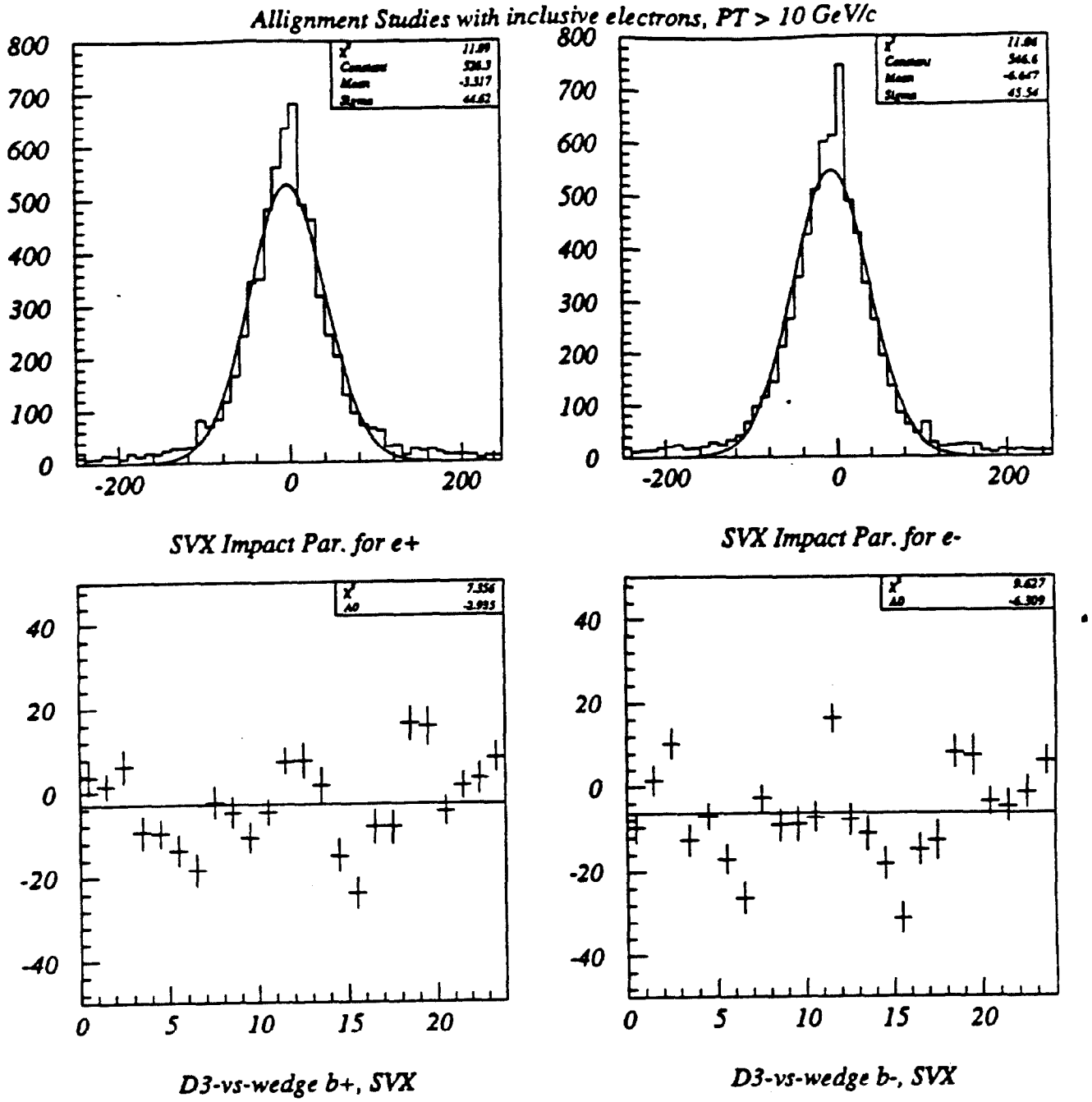

residuals PT>21 GeV
Entries 1846
Mean 0.9101E-04
RMS 0.2989E-02
UDFLW 0.0000E+00
OVFLW 0.0000E+00
χ² 3.246
Constant 239.0 ± 8.691
Mean 0.2798E-04 ± 0.3390E-04
Sigma 0.1373E-02 ± 0.3558E-04
280
240
200
160
120
80
40
0
-0.02 -0.015 -0.01 -0.005 0 0.005 0.01 0.015 0.02
RES2

Figure 84



Impact parameter distributions for electrons/positrons in *cm*. The impact parameter is computed with respect to the beam position, using SVX information.

a) positrons only b) electrons only c) positrons vs wedge number d) electrons vs wedge number

Figure 85a,b,c,d

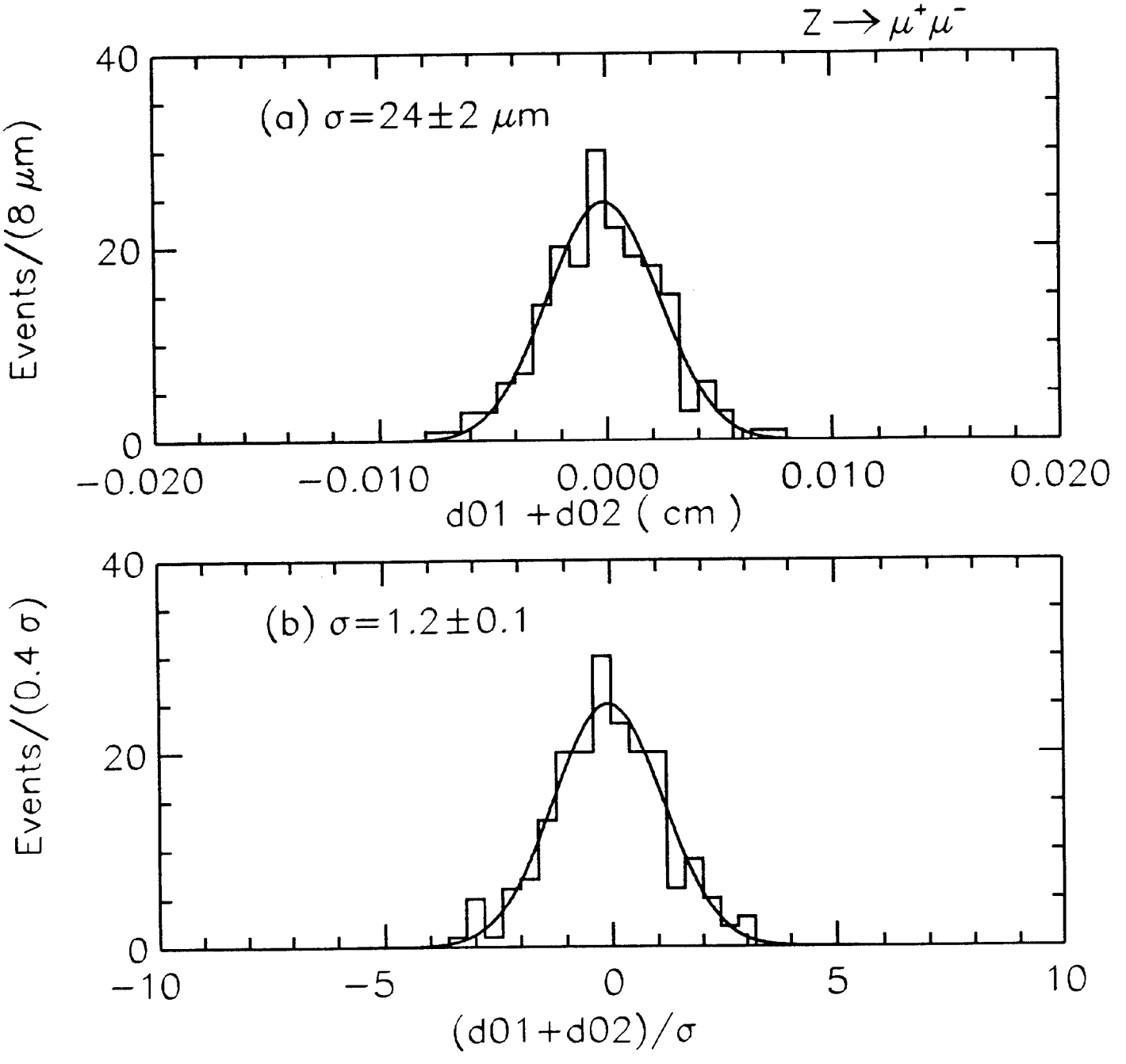

$Z \rightarrow \mu^+\mu^-$
(a) $\sigma = 24 \pm 2$ μm
Events/(8 μm)
40
20
0
−0.020
−0.010
0.000
0.010
0.020
d01 +d02 (cm)
(b) $\sigma = 1.2 \pm 0.1$
Events/(0.4 σ)
40
20
0
−10
−5
0
5
10
(d01+d02)/σ

Figure 86